REVIEWS

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Reconfigurable devices based on two-dimensional materials for logic and analog applications

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Abstract: In recent years, as the dimensions of the conventional semiconductor technology is approaching the physical limits, while the multifunction circuits are restricted by the relatively fixed characteristics of the traditional metal–oxide–semiconductor field-effect transistors, reconfigurable devices that can realize reconfigurable characteristics and multiple functions at device level have been seen as a promising method to improve integration density and reduce power consumption. Owing to the ultrathin structure, effective control of the electronic characteristics and ability to modulate structural defects, two-dimensional (2D) materials have been widely used to fabricate reconfigurable devices. In this review, we summarize the working principles and related logic applications of reconfigurable devices based on 2D materials, including generating tunable anti-ambipolar responses and demonstrating nonvolatile operations. Furthermore, we discuss the analog signal processing applications of anti-ambipolar transistors and the artificial intelligence hardware implementations based on reconfigurable transistors and memristors, respectively, therefore highlighting the outstanding advantages of reconfigurable devices in footprint, energy consumption and performance. Finally, we discuss the challenges of the 2D materials-based reconfigurable devices.

Key words: two-dimensional materials; reconfigurable devices; anti-ambipolar characteristics; nonvolatile devices; artificial intelligence hardware

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1. Introduction

In the past few decades, the semiconductor technology has undergone remarkable development and transformation since the silicon began to be widely studied as a semiconductor material in the mid-20th century, which results in the great success in communication, Internet and other high technology industries. On the one hand, since the first transistor was invented in 1948, the size of transistors has been dramatically decreased due to the improvement of manufacturing processes, materials and the revolution of field-effect transistor (FET) structures from planar transistor to Fin-FET and gate-all-around FET[1]. On the other hand, the integration density of integrated circuits has developed rapidly following the Moore's law, which enables the fabrication of large-scale integration and even ultra-large-scale integration, thus accelerating the development of computers, smartphones, microprocessors and other electronic products.

However, several limitations have appeared in recent years as the semiconductor technology moving towards submicron scale. Firstly, Moore's law is approaching the physical limit when the size of semiconductor devices decreases under 10 nm, which also causes the challenges in manufacturing process, short-channel effect and reliability of traditional transistors[2, 3], whereas the emerging advanced materials and devices bring the issues of compatibility, design complexity and manufacturing cost. In addition, the increase of leakage current results in the issue of trade-off between power consumption, noise margin and performance requirements[4].

To avoid the limitations caused by the size of semiconductor devices, realizing reconfigurable and multiple functions in the same circuit has been explored as another way to improve integration density and performance of integrated circuits. So far, complementary metal–oxide–semiconductor (CMOS) technologies have already been used to fabricate scalable multifunctional circuits and flexible electronics[5, 6], which were designed to complete complex logic or analog functions in a single circuit. However, the field-effect characteristics in the traditional metal–oxide–semiconductor FET (MOSFET) are limited and relatively fixed because the electrical properties and carrier transport in the conventional semiconductor materials are often hardly to control. As a result, reconfigurable circuits based on traditional MOSFETs require additional circuits that consist of many electronic components to achieve reconfigurability[7], which lead to complicating the system design and fabrication process as well as substantial power consumption.

Instead, reconfigurable devices that can realize reconfigurable characteristics and multiple functions at device level provides a method to overcome the challenges above. As an emerging semiconductor device, reconfigurable device can achieve real-time and tunable reconfigurability of its properties according to practical demands, such as polarity-switching and control over transfer characteristics. Therefore, com-

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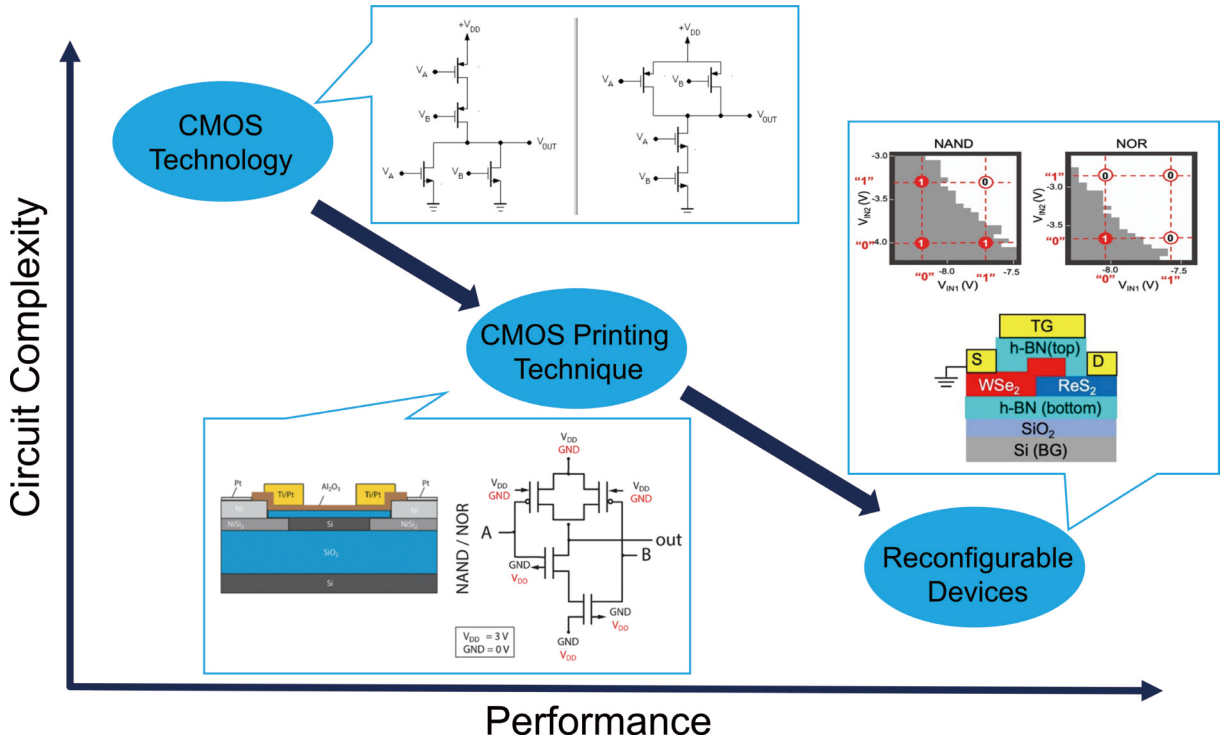

Fig. 1. (Color online) The comparison of the circuit complexity and performance of diverse technologies in implementing the NAND/NOR logic gates circuit. Conventional CMOS technologies are unable to realize both NAND and NOR operations within a single circuit due to the fixed polarity of MOSFETs. Compared to the fixed polarity of CMOS transistors, a CMOS printing technique[6] was used to integrate intrinsic silicon nanowires to construct transistors capable of being programmed as either n-type or p-type. Consequently, utilizing only four transistors allows for the fabrication of a reconfigurable NAND/NOR circuit. Moreover, the output anti-ambipolar characteristics of a reconfigurable dual-gated transistor[8] based on 2D n-ReS_2/p-WSe_2 heterojunction are able to be controlled by the input voltages, therefore a single transistor can accomplish all the two-input logic operations including NAND and NOR, thereby significantly reducing the circuit complexity and enhancing the functionality of circuits.

pared to traditional CMOS technologies that use unipolar transistors, using reconfigurable devices to achieve the same circuit functions can significantly reduce the usage of devices and other components as well as the power consumption and footprint. For instance, Fig. 1 depicts a comparison of the circuit complexity and performance of CMOS technology, CMOS printing technique[6] and reconfigurable device[8] in implementing the NAND/NOR logic gates circuit. As the improvement of the reconfigurable functionality of devices, there is a significant enhancement of circuit performance and reduction of circuit complexity.

Currently, two-dimensional (2D) materials are the main candidates for reconfigurable device fabrication. Since the monolayer graphene was first fabricated in 2004, 2D materials have attracted significant attention all over the world[9]. Different 2D materials also have been widely studied in the fields of electronics and optoelectronics due to their unique properties including varying bandgaps and tunable properties, such as graphene, transition metal dichalcogenide (TMDs), hexagonal boron nitride (h-BN), overmetallic oxide and black phosphorus (BP)[10–12]. Firstly, layered 2D materials have an ultrathin structure without any dangling bond, which simplifies the fabrication process of van der Waals heterostructures (vdWHs) and other devices based on 2D materials, as well as enhances the immunity of these devices to the short-channel effects and the thin-body channel of conventional semiconductors[13]. The ultrathin nature of 2D materials also enables effective transport control and injection tunability of both types of carriers, which are the key prerequisites for realizing reconfigurability in the device level. The lack of dangling bond also significantly suppresses the surface recombination and dark current which are very unfavorable to photodetectors[14]. Additionally, the diverse and tunable electrical properties of 2D materials not only make them ideal for various electronical devices, but also allow them to cover a wide range of electromagnetic spectrum responses for photodetection applications[15]. Furthermore, 2D materials allow the modulation of structural defects, such as grain boundaries and point defects, which can tune the intrinsic properties of 2D materials and thus enables the formation/dissolution process of conductive channels that are vital in the switching of high or low resistance state. Expect electrical properties, 2D materials also exhibit outstanding optoelectrical characteristics such as quantum confinement and strong light–matter interactions[16]. Because of these outstanding characteristics, 2D materials hold strong potential in constructing reconfigurable devices and photodetectors. A comparison between 2D reconfigurable device and traditional CMOS transistor is listed in Table 1.

Currently, "top down" and "bottom up" are the main methods for the growth of 2D materials. Traditional "top down" methods like mechanical exfoliation prepare large-area 2D material films by reducing the dimensions of bulk materials, therefore the films can inherit the crystal structures of the bulk materials[17]. Although it is a cheap and efficient method, this approach needs further improvements in crys-

Table 1. The comparison between 2D reconfigurable device and traditional CMOS transistor.

Comparison	2D reconfigurable device	Traditional CMOS transistor
Polarity(n or p type)	Polarity-switchable according to external conditions	Polarity is decided by doping process and is fixed
Electronical properties	Flexible and tunable	Relatively fixed field-effect
Multifunction	Multifunctional in a single device	Limited by fixed electronical properties
Short channel effect	Immune to short channel effect	Limited by short channel effect
Performance	High performance (on/off current ratio, tunability) and low power consumption	Limited by leakage current, large footprint and high power consumption

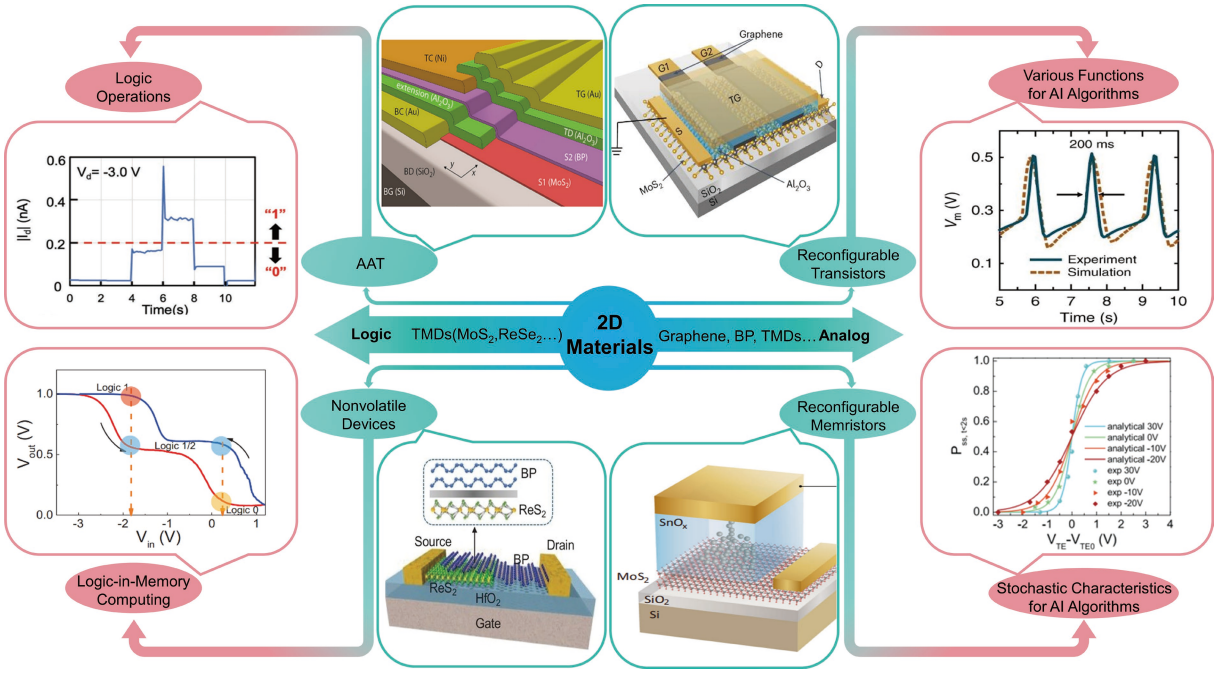

Fig. 2. (Color online) An overview of the recent reconfigurable devices based on 2D materials for logic and analog applications[8, 25, 28–31].

tal quality and large-scale production[18]. "Bottom up" methods are usually used to grow large-scale 2D materials by assembling atoms or molecules, commonly used techniques include chemical vapor deposition, pulsed laser deposition and molecular beam epitaxy[17, 18]. There are two main routes for the growth of 2D materials on substrates: nucleation and growth of a single nucleus and the seamless coalescence of aligned 2D material grains[18]. For instance, through the nucleation and growth of a single nucleus on substrate, wafer-scale graphene monolayers have been successfully synthesized. Wafer-scale h-BN monolayer[19] and centimeter scale MoS_2 film[20] have also been synthesized on tailored substrates through the seamless coalescence of aligned 2D grains on the substrates. These advanced growth methods promote the application of 2D materials in reconfigurable devices.

The unique properties of 2D materials bring them significant advantages in logic and analog applications. For logic applications based on 2D reconfigurable devices, a high on/off current ratio and a rapid switching speed are the most crucial requirements[21]. In order to fulfill these requirements, the relevant 2D materials need to exhibit high carrier mobility and low defect density to improve the switching speed and the stability of the carrier transport, as well as a high carrier concentration to increase the current at the on state. Because of the suitable bandgap and high mobility under short channel condition, TMDs hold great potential for logic applications[22]. For example, MoS_2 films are commonly employed as n-type semiconductor and exhibit relatively high mobility and on/off current ratio[23]. Other TMDs with appropriate bandgap such as $ReSe_2$ and WSe_2 also exhibit much higher on/off ratio, a reconfigurable transistor based on WSe_2 has been reported with an on/off ratio exceeding 10^7 for both n-types and p-types[24].

As for analog applications, high carrier mobility and low defect density are still essential for achieving high performance. However, in certain 2D materials like MoS_2, defects can be modulated to simulate the function of synapses, which is the working principle of some memristors[25]. Another important requirement for analog applications is the precise control over the carrier transport in the devices, which requires the electronical properties in 2D materials can be precisely controlled. Fortunately, the electronic properties and band gap of 2D materials such as BP and TMDs can be controlled by the layers number, heterostructure, external electric field and other methods[26]. For example, the band gap of BP can be adjusted from 0.3 to 2.0 eV by the number of BP layers[21]. In addition, although graphene are not ideal for logic applications due to its low on/off ratio resulting from its zero band gap, utilizing graphene as the contact material offers many significant advantages, including the reduction of the interface states at the graphene-semiconductor interface and the enhanced tunability of electronical properties through the applied input voltages[27].

This review aims to provide an overview of the recent reconfigurable devices based on 2D materials as well as their

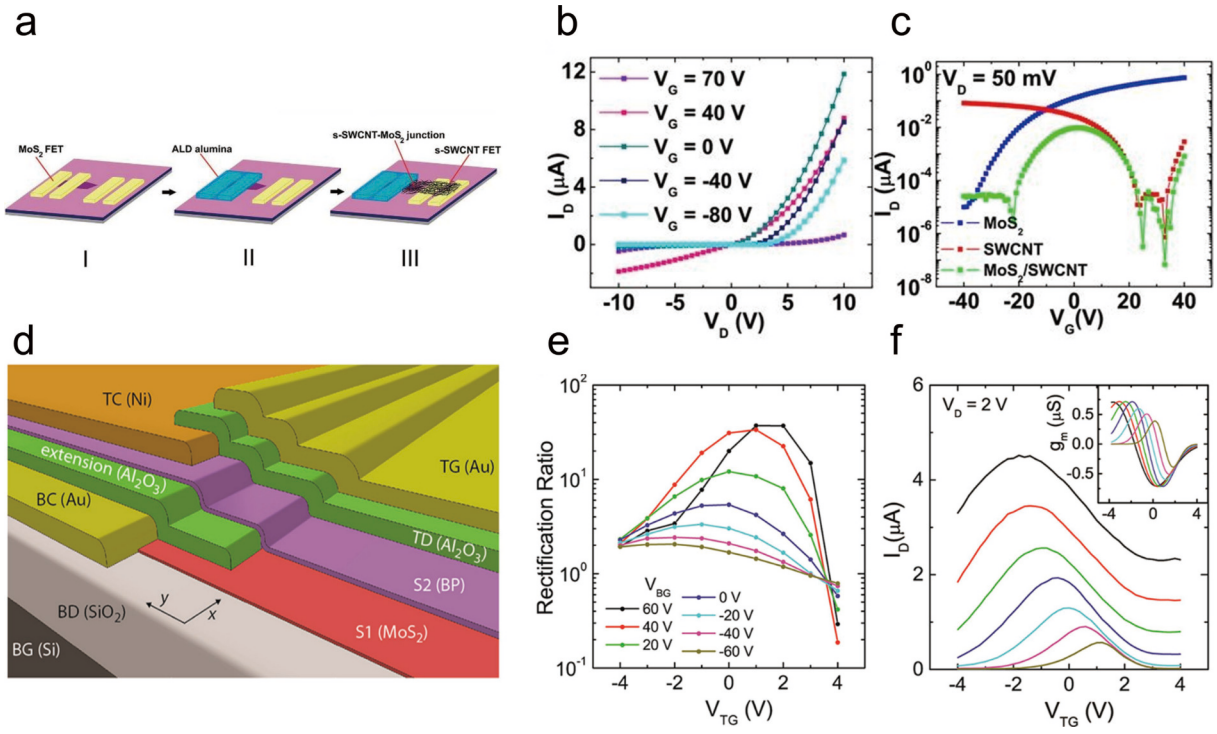

Fig. 3. (Color online) Typical AAT devices. (a) Schematic of the fabrication process, (b) output characteristics, and (c) transfer characteristics of the gate-tunable SWCNT/MoS_2 heterojunction diode[37]. (d) Schematic illustration of the self-aligned heterojunction transistor. (e) The rectification ratios of the BP/MoS_2 at different bottom-gate bias (V_{BG}) values. (f) I_D–V_{TG} characteristics of the heterojunction transistor at different V_{BG}. The inset in (f) shows the variation in transconductance[28].

logic and analog applications that have been reported in recent years. The structure of this review is outlined in Fig. 2. We will present these devices in terms of both logic and analog applications. As for the devices that are used in logic applications, we will introduce two categories of devices that can generate tunable anti-ambipolar characteristics and demonstrate nonvolatile operations at the device-level, we will also analyze the working principle, output characteristics and related logic applications, including logic operations and logic-in-memory computing. On the other hand, we will summarize the anti-ambipolar transistors (AATs), reconfigurable transistors and reconfigurable memristors that are applied to analog applications, such as analog signal processing circuits and the emerging artificial intelligence (AI) hardware implementations. Finally, we will discuss the challenges and outlook of the 2D reconfigurable devices.

2. 2D reconfigurable devices for logic applications

By controlling the gate voltage of a traditional MOSFET, we can easily change the working regions of a MOSFET, thereby obtaining the switching of the on/off states in the output currents. Therefore, MOSFETs can be used to implement simple logic circuits such as electronic switches and logic gates. However, when it comes to more complicated logic functions, CMOS technologies have to use a large number of MOSFETs, which causes large parasitic resistance and high delay of the circuit. The increase of static leakage current also can't be neglected.

Compared to MOSFETs, reconfigurable devices have more flexible transport properties and scalability due to the advantages of 2D materials, which make them well suited for complicated logic circuits. In this Section, we will review two commonly used reconfigurable devices in logic circuits, AATs and nonvolatile memories, as well as describing their respective functions and applications.

2.1. 2D AAT devices for reconfigurable logic circuits

Utilizing the weak van der Waals interaction between 2D materials, vdWHs can be built through the stacking of different layered 2D materials, which avoids the issues of lattice mismatch and interface defects between different materials, but also preserves the unique properties of each layer[32–34]. Therefore, semiconductor devices based on 2D vdWHs exhibit numerous unique and promising properties in the fields of electronics and photonics[35]. Among them, anti-ambipolar characteristic is one of the most attractive properties, which refers to the Λ-shaped transfer curve of the heterojunctions, and can be used to achieve advanced logic functions[29, 36] and neuromorphic computation.

The first AAT device with gate-tunability was reported in 2013[37]. In this study, a gate-tunable p–n heterojunction diode was created by semiconducting single-walled carbon nanotubes (SWCNTs) and single-layer MoS_2, which was used as p-type and n-type semiconductor layer, respectively. Fig. 3(a) shows the fabrication process and structure of the SWCNT/MoS_2 heterojunction diode. By applying a bias voltage V_G to the gate electrode of the diode, the electrostatic doping of the semiconductor layers can be controlled by the applied V_G due to the atomically thin nature of 2D layered materials. Therefore, the charge transport behavior of this p–n heterojunction shows a wide tunability from nearly insulating to highly rectifying, as shown in Fig. 3(b). Moreover, within a certain range of V_G, the transfer characteristics of the device shows an anti-ambipolar behavior (Fig. 3(c)) that can be qualitatively explained as originating from the channel consisting of p-type and n-type semiconductors in series, which

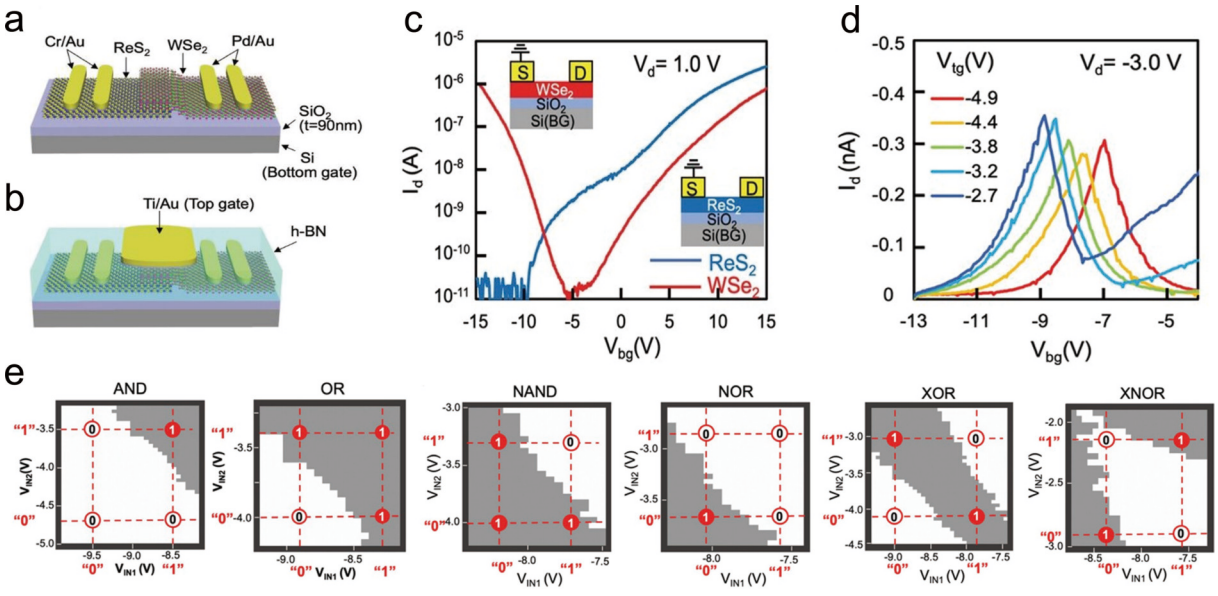

Fig. 4. (Color online) 2D reconfigurable AAT devices applied to reconfigurable logic circuits. Schematic illustrations of (a) the bottom-gated ReS_2/WSe_2 AAT and (b) the dual-gated ReS_2/WSe_2 AAT. (c) The transfer curves of the ReS_2-FET (blue) and WSe_2-FET (red) with V_d at 1.0 V. (d) The transfer characteristics of the dual-gated ReS_2/WSe_2 AAT. (e) The two-input logic operations are able to be demonstrated in a single dual-gated ReS_2/WSe_2 AAT[8].

also has a high on/off current ratios up to 10^4.

In the next few years, the AAT devices based on 2D vdWHs have witnessed rapid development, various combinations of 2D materials were used to build AATs such as p-WSe_2/n-MoS_2 vdWH transistor[38, 39], p-WSe_2/n-WS_2 vdWH transistor[40], p-BP/n-MoS_2 heterojunction[41], SnS_2/WSe_2 heterojunction-based AAT[42]. However, there was still a lack of a method to simultaneously achieve the fabrication of short channel and large footprint devices, and the relative alignment between different layers in 2D vdWHs was restricted by the diffraction resolution of transfer and alignment techniques[28].

In 2018, a self-aligned, semi-vertical and source-gated architecture[28] was reported to overcome these shortcomings and fabricate a p-BP/n-MoS_2 heterojunction transistor with a short channel length of less than 150 nm, Fig. 3(d) shows the schematic illustration of the self-aligned heterojunction transistor. The asymmetry architecture in the transistor allows the source-gated configuration where the bottom electrode (drain) is biased while the overlapping electrode (source) is grounded, which results in an extra depletion region near the drain contact and therefore improves current saturation and reduces short channel effect. Fig. 3(e) shows the rectification ratio of the BP/MoS_2 at different bottom-gate bias (V_{BG}) values.

Moreover, in the dual-gated architecture, due to the screen effect of the MoS_2 layer on the bottom gate, the BP layer is controlled only by the top gate. Similarly, the overlapped MoS_2 layer underneath BP is controlled only by the bottom gate because of the screening of top gate, while the nonoverlapped MoS_2 layer is controlled by both gates. This architecture provides controlled and improved electrostatic doping as well as the gate-tunability of the heterojunction, thus enables the control of all characteristics of the anti-ambipolar response. As shown in Fig. 3(f), the anti-ambipolar response of the heterojunction transistor can be tuned by V_{BG}, which is also reproduced by finite-element simulation. These characteristics give this hereoterjunction transistor a unique advantage in signal processing applications and scalable frequency amplifiers and mixers.

Negative differential resistance (NDR) devices that have a high peak-to-valley ratio (PVR) have been regarded as the key components of logic circuits. Compared with the NDR devices that need to be operated in a low temperature environment, AATs can exhibit anti-ambipolar characteristic that is similar to the NDR behavior and achieve high PVRs at room temperature[43]. Therefore, AATs hold a great promise for various kinds of logic circuits, such as reconfigurable logic gate operations[8, 44] and multi-valued logic (MVL) circuits[29, 37, 38, 45, 46].

Single-electron transistors[47] and CMOS technology have been used to realize multiple logic gate operations, but they need to face the issues of cryogenic temperature environment and extensive use of transistors, respectively. In contrast, there were numerous AAT devices reported to achieve reconfigurable logic gate operations in a single device at room temperature. In 2022, A dual-gate organic AAT was fabricated to achieve reconfigurable five two-input logic operations[44].

In 2023, a dual-gated AAT based on 2D ReS_2/WSe_2 heterojunction was fabricated to achieve all the reconfigurable two-input logic operations in a single transistor[8], where WSe_2 and ReS_2 were used as p-type and n-type semiconductors in the heterojunction, respectively. Figs. 4(a) and 4(b) show the schematic illustration of a bottom-gated AAT and a dual-gated AAT where the top electrode covers the channel area, respectively. Fig. 4(c) shows the transfer curve of a ReS_2-FET (blue) that exhibits n-type characteristics and a WSe_2-FET (red) that exhibits ambipolar characteristics. Moreover, compared with the threshold voltage of n-type ReS_2-FET, WSe_2-FET's threshold voltage of the p-type condition was much higher, which enables the dual-gated AAT to demonstrate anti-ambipolar characteristics when these two FETs are both in the on state. Fig. 4(d) shows the Λ-shaped anti-ambipolar

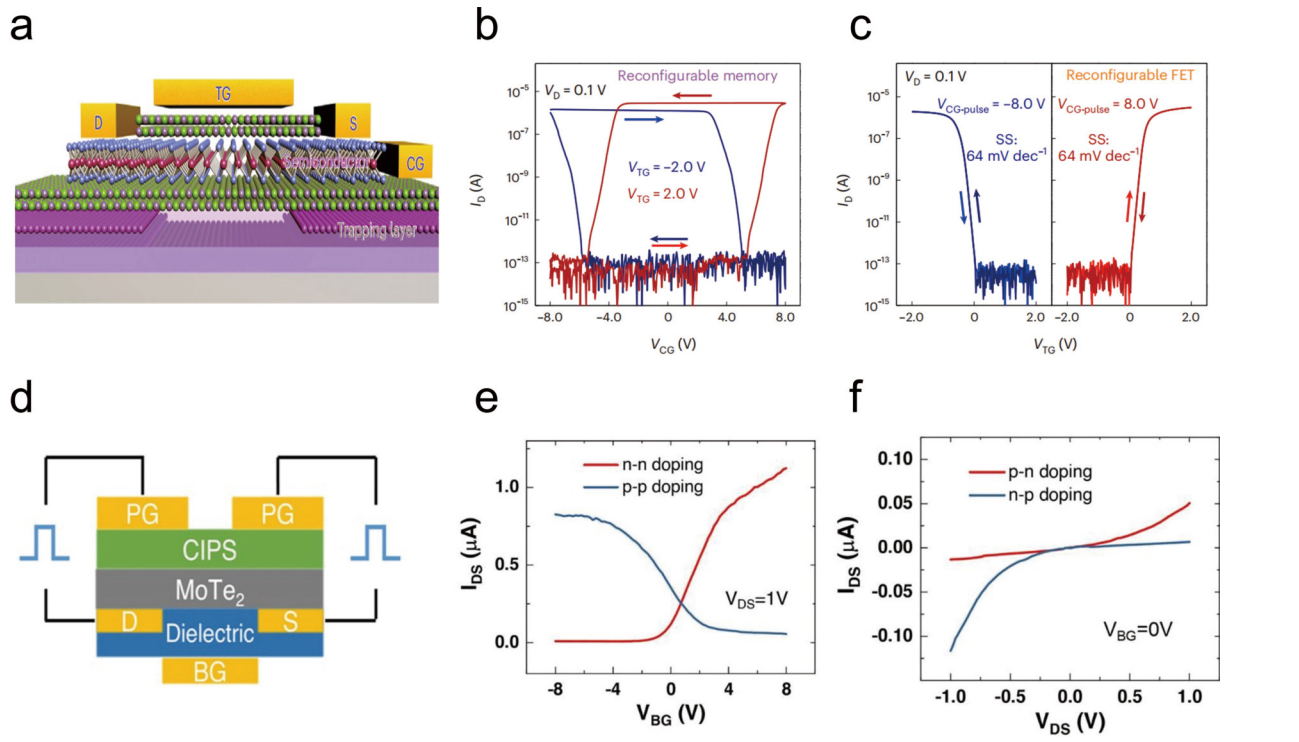

Fig. 5. (Color online) Nonvolatile reconfigurable multifunctional devices. (a) The schematic of the partial-floating-gate FET. The transfer characteristics of the partial-floating-gate FET acquired in (b) the reconfigurable memory mode and (c) the reconfigurable FET mode[72]. (d) The schematic of the reconfigurable transistor based on ferroelectric $CuInP_2S_6/MoTe_2$ heterostructure. (e) Transfer curves of the $CuInP_2S_6/MoTe_2$ heterostructure transistor in symmetrically programming state (p–p and n–n doping). (f) Output curves of the transistor in asymmetrically programming state (p–n and n–p doping)[73].

transfer curves of the ReS_2/WSe_2 AAT with different top-gate voltage (V_{tg}) while the drain bias (V_d) is fixed at −3 V. It should be noted that the peak voltage is clearly dependent on V_{tg} while the peak width remains almost the same (~1.1 V) due to the WSe_2-FET's ambipolar characteristics. These unique properties are important for the implementation of reconfigurable logic operations. Therefore, by optimizing the input voltages, all the two-input logic operations can be demonstrated in a single dual-gated AAT, including AND, OR, XOR, NAND, NOR, and XNOR (Fig. 4(e)), which is significant for simplifying circuits design and improving integration density.

MVL circuits can benefit the integration density by increasing the number of logic states[48], which are significant for next-generation high performance digital electronics[49]. As one of the most significant applications of the MVL circuits, the first ternary inverter based on 2D vdWH was reported in 2016 using a MoS_2/WSe_2 heterojunction[38]. This ternary inverter can be qualitatively equivalent to a WSe_2-FET in series with a MoS_2/WSe_2 Hetero-FET, where the MoS_2/WSe_2 Hetero-FET exhibits anti-ambipolar characteristics. After that, many studies have reported ternary inverters based on different AATs, such as organic AATs[45, 50], BP/ReS_2 heterojunction transistors[46], BP/MoS_2 heterojunction transistors[41], photosensitive graphene p–n junction AATs[51] and $MoTe_2/MoS_2$ heterojunction transistors with photoinduced doping[52]. In 2020, a 2D vdWH based on BP and ReS_2[29] was created to demonstrate nonvolatile ternary logic operations for the first time. In addition to ternary inverters, other MVL applications also have been realized by using AATs, including quaternary inverters[53, 54], ternary latches and static random-access memory[55] based on AATs with M-shaped transfer curves.

2.2. 2D reconfigurable nonvolatile devices for logic-in-memory computing

To overcome the bottleneck of the conventional von Neumann computing architecture, where the computing and storage of increasing data are separated and thus causing the issues of significant latency and energy consumption[4], nonvolatile devices for in-memory computing that can realize data processing and storage in the same device have attracted intensive attention[29, 56]. By shortening the distance of data transmission, nonvolatile devices are expected to achieve high efficient data computing and processing with lower energy consumption[57]. Because of the dangling-bond-free surface, atomical thickness, and diversity of energy band structures[58–60], 2D materials are promising candidates for the building of nonvolatile reconfigurable devices, including multifunctional devices[61–64], nonvolatile memory[65–69] and logic-in-memory computing devices[29, 70, 71].

In addition to realizing specific reconfigurable and tunable function in a single device, another approach to improve the integration intensity is to realize nonvolatile multifunction in the same device, thus allowing these devices to achieve diverse functions or change working modes according to different external conditions. For example, the polarity of a traditional CMOS transistor can't be changed after fabrication due to the physical doping of the drain/source regions, but the polarity of 2D reconfigurable transistors can be switched during run-time due to the electrostatic doping nature of 2D materials[73] or the photo-induced doping[74]. Moreover, the design of nonvolatile reconfiguration allows

lower energy consumption and higher reliability of these devices. Previous 2D nonvolatile reconfigurable devices were mostly built on floating-gate structures using MoS_2[75], WSe_2[76], $MoS_2/MoTe_2$[77] as channel materials, in which the floating gate controls the charge storage layer.

However, in the devices above, different operations were always controlled by the same terminal, resulting in the issues of reliability and versatility. In 2022, a 2D graphene/hBN/WSe_2 heterostructure transistor was fabricated to perform as reconfigurable nonvolatile memory and polarity-switchable FET with a partial floating-gate serving as the charge-trapping layer[72]. Fig. 5(a) shows the schematic of the partial-floating-gate FET (PFGFET), where the partial floating-gate (CG) and top field (TG) gate provide efficient electronic control of the contact region and WSe_2 channel, respectively. Fig. 5(b) shows the transfer curves of the PFGFET set in reconfigurable memory mode, which are obtained by sweeping the CG voltage (V_{CG}) forward and backward between −8 and 8 V with V_D = 0.1 V and V_{TG} = ±0.2 V. The PFGFET can exhibit both n-type (V_{TG} = 2 V) memory and p-type (V_{TG} = −2 V) memory with a reduced V_{CG} and an erase/program ratio of 10^8 for both modes. This device can also be operated in polarity-switchable FET mode, when TG and CG act as input and trigger terminal, respectively. The transport characteristics in Fig. 5(c) are obtained by sweeping V_{TG} between −2 and 2 V after applying a V_{CG} pulse of ±8 V to the PFGFET, the curve in the left part exhibit p-type behavior ($V_{CG\text{-}pulse}$ = −8 V) while the right one shows n-type behavior ($V_{CG\text{-}pulse}$ = 8 V). Moreover, both transport behaviors of n-type and p-type mode show a small hysteresis and high on/off ratio about 10^8. These outstanding characteristics make the PFGFET suitable for many logic-in-memory applications including linear/nonlinear logic gates and half-adder, which are attributed to the partial floating gate that significantly improves the carrier injection in contact region, where a sufficiently negative $V_{CG\text{-}pulse}$ can simultaneously induce a small hole Schottky barrier and a large electron Schottky barrier at the interface of metal/semiconductor, then resulting in a high on/off ratio.

The stable spontaneous polarization nature of ferroelectric materials enables ferroelectric FETs (FeFETs) based on the stack of ferroelectric/semiconductor to achieve different functions with nonvolatile properties, including reconfigurable memory[78–80], optoelectronic photodetectors[81, 82] and electronic/optoelectronic synapses[83, 84]. Zhao *et al.* built a nonvolatile reconfigurable transistor based on 2D ferroelectric $CuInP_2S_6/MoTe_2$ heterostructures in 2021[73], and the structure of the device is shown in Fig. 5(d). The electrodes above the CIPS and below the dielectric layer serve as the program gates (PG) and back gate (BG), respectively. The nonvolatile properties are attributed to the ferroelectric dipoles in CIPS that contribute to the doping of electron/hole in $MoTe_2$, which can be maintained after cutting off power supply. To be specific, the polarization condition in the CIPS maintained almost the same in 1 h during the retention test. Moreover, the contacts of drain and source are sandwiched between the channel and BG, resulting in the screen of the field from BG, thus providing better individual electrostatic control of this device. When the device is operated in the nonvolatile reconfigurable transistor mode, the doping conditions of the drain and source contacts are programmed individually. Fig. 5(e) shows the transfer curves of the reconfigurable transistor with V_{DS} = 1 V in symmetrically programming state (p–p and n–n doping), where both contacts act as the reservoirs of the carriers, thus exhibiting p-type or n-type unipolar behavior. In contrast, Fig. 5(f) shows the output curves of the transistor with V_{BG} = 0 V when the contacts are programmed asymmetrically (p–n and n–p doping), exhibiting rectifying behaviors in both conditions. What's more, this device can also be used to exhibit a series of tunable photo response, where p–p doping and n–n doping states generate positive and negative photocurrent, respectively, whereas the asymmetrical states can exhibit strong photovoltaic effect. These nonvolatile reconfigurable and optoelectronic characteristics of the device have a great potential in future computing and sensing system implementations.

There are also other approaches used to achieve 2D nonvolatile reconfigurable devices. In 2023, using a photoinduced trapping mechanism that can drive photoexcited carriers into the interface of h-BN/SiO_2 and Si substrate, a reconfigurable transistor based on h-BN/$ReSe_2$/h-BN heterostructure was reported with nonvolatile tunable polarity[85], which can be used to create logic circuits and emulate synaptic functions. An effective-gate-voltage-programmed graded-doping strategy[7] was used to fabricate a single-gate $MoTe_2$ transistor in the same year, which can be programmed to different operation modes including polarity-switchable diodes, in-memory logic gates and electronic synapses. A three-gate reconfigurable FET was also proposed as synaptic devices, which allowed the NOR/XNOR operations in the binary neural network[86].

Logic-in-memory computing, which refers to the integration of logic operations in nonvolatile memory units, has a great advantage in saving transistors and energy consumption for nonvolatile logic applications. So far, various device structures based on 2D materials have been used to realize logic-in-memory computing, such as vdWHs[29, 72, 87], floating-gate FETs[71, 75, 88, 89] and FeFETs[70, 80].

In 2023, a middle-floating-gate FET (MFGFET) was fabricated by Sheng *et al.* using a 2D WSe_2/h-BN/graphene vdWH[71]. Fig. 6(a) depicts the schematic of the MFGFET based on WSe_2/h-BN/graphene heterostructure, where WSe_2, h-BN and multilayer graphene serves as the channel material, tunneling layer and floating gate, respectively. In particular, the graphene floating gate is aligned with the middle of the WSe_2 channel in the middle-floating-gate architecture, which allows the central part of the channel to be controlled by the floating gate. Therefore, by controlling the voltages of the middle floating gate (V_{MFG}), control gate (V_{CG}), drain and source (V_{DS}), the polarity and current level of the MFGFET can be adjusted between n-type and ambipolar behavior. Taking advantages of these properties, reconfigurable logic operations of AND (V_{DS} = 0.5 V) and XNOR (V_{DS} = 3 V) can be achieved in a single MFGFET, where V_{CG} and V_{MFG} act as input signals IN1 and IN2, current I_{DS} acts as output signal I_{OUT} (Fig. 6(b)). Moreover, since the charge-trapping function of the middle floating gate, the reconfigurable logic functions can be integrated into the nonvolatile memory with the trapped charges playing the role of stored logic operand. Fig. 6(c) shows the nonvolatile behavior of the MFGFET, where exists a memory window in the transfer curves with the V_{CG} sweeping forth and back, and a high erase/program current ratio up to 10^4 at V_{CG} = 0 V. By programming/erasing

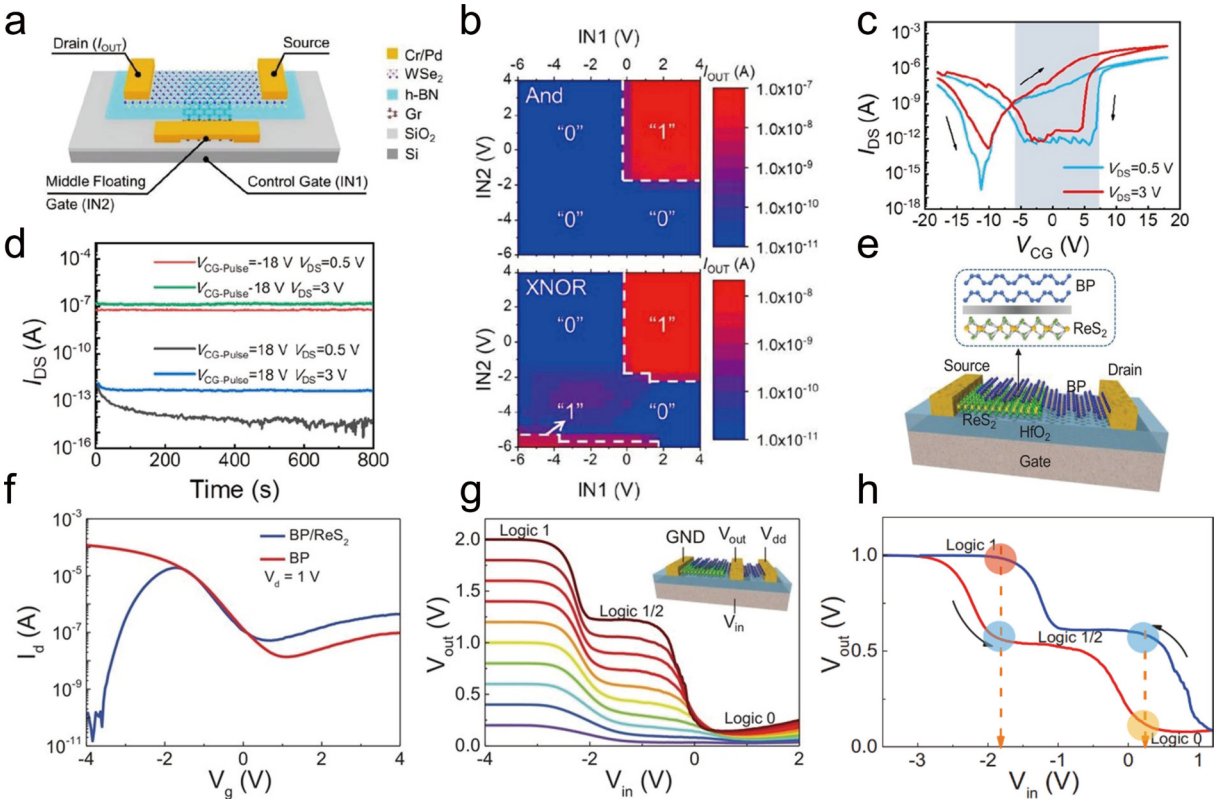

Fig. 6. (Color online) Nonvolatile devices used for logic-in-memory computing. (a) The schematic of the middle-floating-gate FET (MFGFET) based on WSe_2/h-BN/graphene vdWH. (b) Reconfigurable logic operations achieved in a single MFGFET. (c) The transfer curves of the MFGFET show a memory window. (d) The retention characteristics of the MFGFET[71]. (e) Schematic illustration of the BP/ReS_2 heterostructure device. (f) The transfer curves of the BP-FET (blue) and the BP/ReS_2-FET (red), respectively. (g) The output characteristics of the ternary logic circuit based on a BP/ReS_2 heterojunction device. (h) The double swept voltage transfer characteristics of the ternary logic inverter circuit[29].

the device with a $V_{CG\text{-}pulse}$ and then reading the current states, the retention characteristics of the MFGFET are shown in Fig. 6(d), where all the current states retain well within 800 s, thus showing a reliable data storage capacity.

In 2019, using a graphene floating gate surrounded by dielectric layers to store charges, a dual-gate floating-gate FET[88] with a MoS_2 channel was fabricated to achieve photo-switching logic operations (OR/AND) and *in situ* memory in a single device. Except serving as the input signals in the logic operation mode, the voltages of dual gate can also be used to carry out write operations, which can store the logic states in the floating gate. Similar functions can also be realized by a 2D dual-gate transistor based on the stack of Al_2O_3/HfO_2/Al_2O_3[90], which serves as the dielectric layer as well as trapping or releasing charges.

Utilizing the electrical hysteresis effect of ferroelectrics, FeFETs can be used to realize nonvolatile memory by substituting ferroelectrics for oxides as the dielectric layer[91]. In 2022, a dual-gate FeFET based on MoS_2 and $MoTe_2$[70] was explored to form nonvolatile logic gates (including AND, OR, XNOR) for both digital and analog in-memory computing. In 2020, more advanced logic functions with memory ability including flip-flop and d-type latch were carried out by unipolar memristors for the first time based on MoS_2/graphene/$HfSe_{2-x}O_x$ vdWHs[87].

Except traditional binary logic operations, MVL circuits can also be realized by nonvolatile devices. In 2020, based on 2D BP/ReS_2 vdWHs, an anti-ambipolar device was demonstrated for nonvolatile ternary logic operations[29]. Fig. 6(e) shows the schematic of the BP/ReS_2 heterojunction device, which is built on a HfO_2-coverd silicon substrate. Fig. 6(f) shows the transfer curves of the BP-FET and the BP/ReS_2-FET with the drain voltage fixed at 1 V. It's worth noting that the transfer curve of the BP/ReS_2-FET exists a negative transconductance region, which derives from the band-to-band n-type hole tunneling caused by the drain bias pulling down the energy band of BP. Therefore, ternary logic circuits can be achieved by a BP-FET and a BP/ReS_2-FET in series. Fig. 6(g) shows the output characteristics of the ternary logic circuit based on a BP/ReS_2 heterojunction device with V_{dd} increasing from 0.1 to 2 V, and the inset shows the schematic diagram of the circuit. This circuit can demonstrate three distinct logic states including "1", "0" and an additional "1/2". Moreover, due to the natural oxidation of the BP layer, there is an ultrathin phosphorus oxide (PO_x) layer on the surface, which serves as the band–band tunneling layer and the charge trapping layer at the same time, thus resulting in an obvious hysteresis and memory states under the condition of double voltage sweep (Fig. 6(h)). Utilizing these characteristics, this device can be used to demonstrate nonvolatile ternary logic operations with low energy consumption and small footprint.

3. 2D reconfigurable devices for analog applications

Apart from the logic circuits that compute discrete signals, analog circuits that process continuous signals are also essential in practical applications. However, with the increase

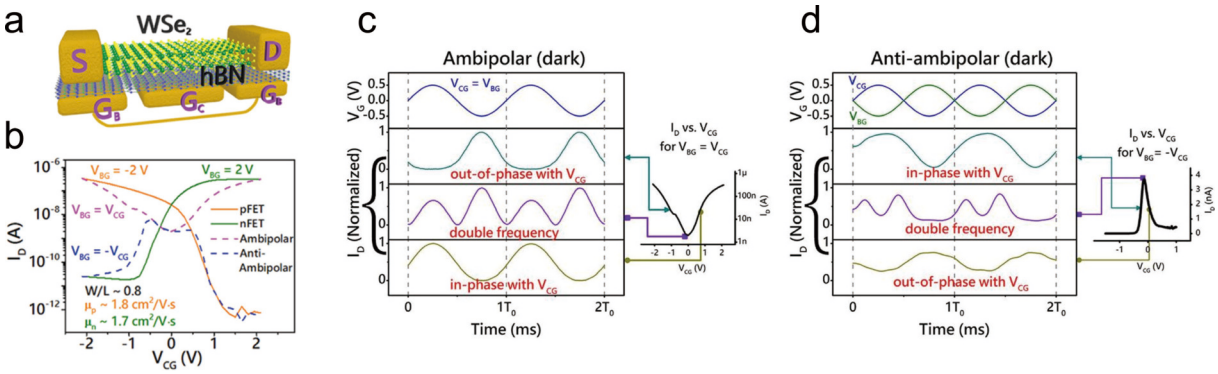

Fig. 7. (Color online) 2D reconfigurable AAT devices applied to analog signal processing. (a) The three-dimensional schematic of the dual-gate WSe_2 transistor. (b) The transfer curves and the respective biasing configurations of the four modes (n-FET, p-FET, ambipolar, and anti-ambipolar) of the WSe_2 transistor. The frequency and phase operations achieved by the WSe_2 transistor in the condition of dark environment and (c) ambipolar or (d) anti-ambipolar modes[36].

of the scale and complexity of circuits, analog circuits based on traditional CMOS technology are facing the issues of noise and the trade-off between performance and power consumption.

With special designs, reconfigurable devices based on 2D materials are able to generate multiple transfer characteristics with precise tunability, which makes them more flexible in different analog applications. In this Section, we will review the analog signal processing applications of AATs. Furthermore, we will discuss the 2D reconfigurable transistors and memristors that have been used to implement various AI hardware.

3.1. 2D reconfigurable AATs for analog signal processing

As mentioned in Section 2.1, the Λ-shaped transfer curves of AATs enable both positive and negative transconductances to be exhibited in a single device. Moreover, the architecture of dual-gate provides controllable electrostatic doping and the gate-tunability of the AAT, thus enables the control of the anti-ambipolar response[28]. These characteristics bring AATs unique advantages in analog signal processing applications[32], such as phase shift keying, frequency multipliers and frequency mixing.

Previous frequency multipliers usually consisted of nonlinear electronic components. In 2020, a frequency doubling circuit was demonstrated based on AAT devices, where the device is built from the 2D $MoTe_2/MoS_2$ heterojunction[92]. This frequency doubler consisting of only one device can operate well within 3 kHz, which significantly reduce the number of transistors that needed to achieve frequency multipliers compared to conventional CMOS methods. Furthermore, a graphene-bridge based AAT device was demonstrated to achieve a frequency tripler in 2023[93], which used laterally series-connected ambipolar WSe_2/graphene/MoS_2 as the channel of the AAT device that shows N-shaped transfer curves.

Combining the advantages of the ambipolar and anti-ambipolar characteristics can enhance the reconfigurability and tunability for frequency modulation applications. In 2021, a WSe_2 transistor that can exhibit both ambipolar and anti-ambipolar transfer curves was reported for the first time[36], which was built on an ambipolar WSe_2 channel with dual-electrostatic control and source/drain Schottky barriers. Fig. 7(a) shows the three-dimensional schematic of the WSe_2 transistor. A dual-gate structure, G_B and G_C, was used to control the transport of the transistor, which separately decide the polarity of the Schottky barrier and the channel, thus controlling the transfer characteristics. Fig. 7(b) shows the transistor's transfer curves of the four modes (n-FET, p-FET, ambipolar and anti-ambipolar) and the respective biasing configurations, with the mobility of 1.8 and 1.7 $cm^2/(V·s)$ for holes and electrons, respectively. In the condition of dark environment and ambipolar/anti-ambipolar modes, the transistor can achieve frequency and phase operations in the output current waveforms, including double frequency, in-phase and out-of-phase, as shown in Figs. 7(c) and 7(d). It is worthy noted that there was a phase shift of ±90° between the output waveforms of the ambipolar and anti-ambipolar modes. These characteristics of the WSe_2 transistor benefit the analog modulation/encoding schemes and 2/3-bit data transmission as well as reduce fabrication complexity of the AATs.

In addition to frequency multipliers, AAT devices also have been used to implement phase shift keying (PSK) and frequency shift keying (FSK) circuits, which are widely used in the technologies of wireless data transmission, microwave radio and telecommunications. CMOS technologies[94] and 2D ambipolar transistors[95] have already been used to design PSK and FSK circuits. In 2015, an AAT device based on a SWCNT/a-IGZO heterojunction[96] was reported to enable PSK operations that are dependent on the out sine, as well as the FSK operations utilizing the combination of one heterojunction device in series with a load resistor. Using the same WSe_2 transistor and similar circuit configuration[36] can also demonstrate the PSK function. In particular, under the illumination of 532 nm, the transfer curves of the transistor in the anti-ambipolar mode exhibit a significant left shift compared to the dark characteristics.

3.2. 2D reconfigurable transistors for AI hardware implementations

Inspired by the behaviors of the human nervous systems, AI technologies have developed rapidly in recent years and played an important role in neuromorphic computing, which can effectively improve the efficiency and reliability of data processing. Moreover, the hardware implementations of AI algorithms enable the neuromorphic computing at hardware-level, thus avoiding the issues of latency and stability caused by the limitations of network bandwidth and massive

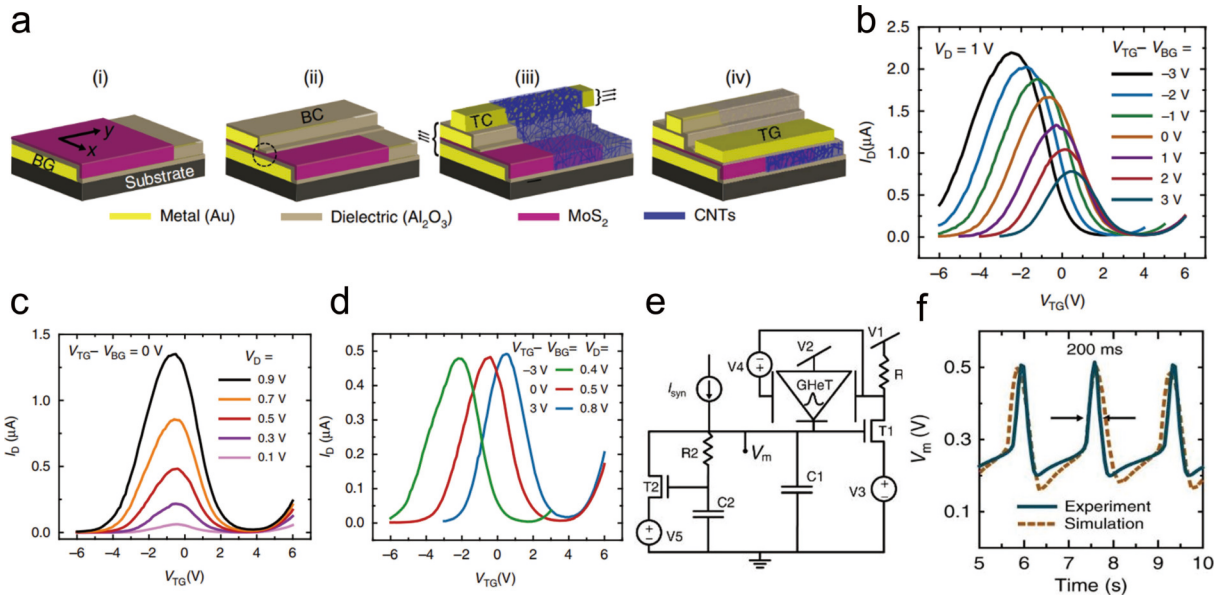

Fig. 8. (Color online) Spiking neuron based on 2D reconfigurable Gaussian heterojunction transistor (GHeT). (a) The fabrication process of the dual-gated GHeT based on SWCNTs/MoS_2 heterojunction. I_D–V_{TG} characteristics of the GHeT shows the control of (b) both sides of the anti-ambipolar response and of the peak position, (c) the height and (d) the peak position. (e) The diagram of the spiking neuron circuit that utilizing only one GHeT. (f) The experiment and simulation results of the GHeT spiking neuron exhibit spiking and resetting behaviors[31].

data. Because of its unique energy band structures and rich electronic properties, 2D materials are strong candidates for devices that can realize reconfigurable analog functions for AI algorithms. Up to now, various 2D reconfigurable transistors have been reported for the hardware implementations of AI algorithms.

Kernel functions, including linear, Gaussian, polynomial and sigmoid functions, are widely used to map input vectors from the origin space into a high-dimensional characteristic space in AI algorithms such as neural networks, support vector machine (SVM) and logistic regression. As one of the most commonly used kernel functions, Gaussian functions are widely used in many AI applications, such as artificial neural networks based on Gaussian synapses[97, 98], spiking neurons for spiking neural networks (SNNs)[31] and SVMs for classification tasks[99]. Although silicon-based CMOS technologies have already been used to build digital and analogue hardware for the generation of Gaussian functions, but they both consist massive transistors and other elements, resulting in large footprint and high power consumption, which makes them impossible to achieve real-time and off-grid applications of AI technologies. Additionally, the additional circuits of CMOS hardware require a large number of transistors and complicated structures, which limits the integration density and scalable implementations of the AI computing systems.

Utilizing the weak electrostatic screening properties[100], AAT devices based on 2D materials can generate gate-tunable and reconfigurable Gaussian response under suitable biases, which is of great importance of the hardware-level neuromorphic computing. So 2D AAT devices have been exploited to generate tunable Gaussian responses in a single device, thus simplifying the hardware implementations of AI applications and the additional circuits.

For example, SNN, which uses discrete spikes and the incorporation of time, can dramatically improve the energy efficiency of neuromorphic computing by mimicking the behaviors of nervous system more graphically[101]. Except CMOS technologies, several approaches have been explored to realize neuromorphic functionality for spiking neurons at device level, such as NbO_x based metal–insulator transition (MIT) devices[102], ultrathin 2D TiO_x nanosheets[103], diffusive memristors[104] and FeFETs[105], but these approaches still face many challenges including limited output swing and incomplete synaptic functions. In 2020, a Gaussian heterojunction transistor (GHeT) was fabricated for spiking neurons implementations based on 2D SWCNTs/MoS_2 heterojunction[31]. Fig. 8(a) shows the fabrication process of the dual-gated GHeT structure, where the monolayer MoS_2 and solution-processed CNT exhibit n-type and ambipolar behavior in this structure, respectively. Moreover, due to the dual-gate, self-aligned structure and electrostatic screening effect, the CNTs can be fully controlled by top gate (TG) and partially controlled by the bottom gate (BG), whereas the monolayer MoS_2 can be fully modulated by the BG and partially modulated by the TG. Therefore, the diversity of current combinations modulated by TG and BG enable the reconfigurability and gate-tunability of the Gaussian response in a single device, Figs. 8(b)–8(d) show the Gaussian curves of the GHeT with controlled anti-ambipolar response, height and peak position under different biasing configuration.

Taking advantages of the tunable Gaussian response of the GHeT, this device can be used to build a circuit-level spiking neuron. The diagram of the full spiking neuron circuit is shown in Fig. 8(e), which consists one GHeT, two n-FETs (T1 and T2) and other elements including capacitors, resistors and voltage sources. The GHeT spiking neuron is able to exhibit spiking and resetting behaviors in both experiments and simulations by emulating the behavior of Na^+ conductance, which is shown in Fig. 8(f). The GHeT device significantly simplifies the structure of the spiking neuron circuits, which enables the scalable SNN applications with lower energy consumption.

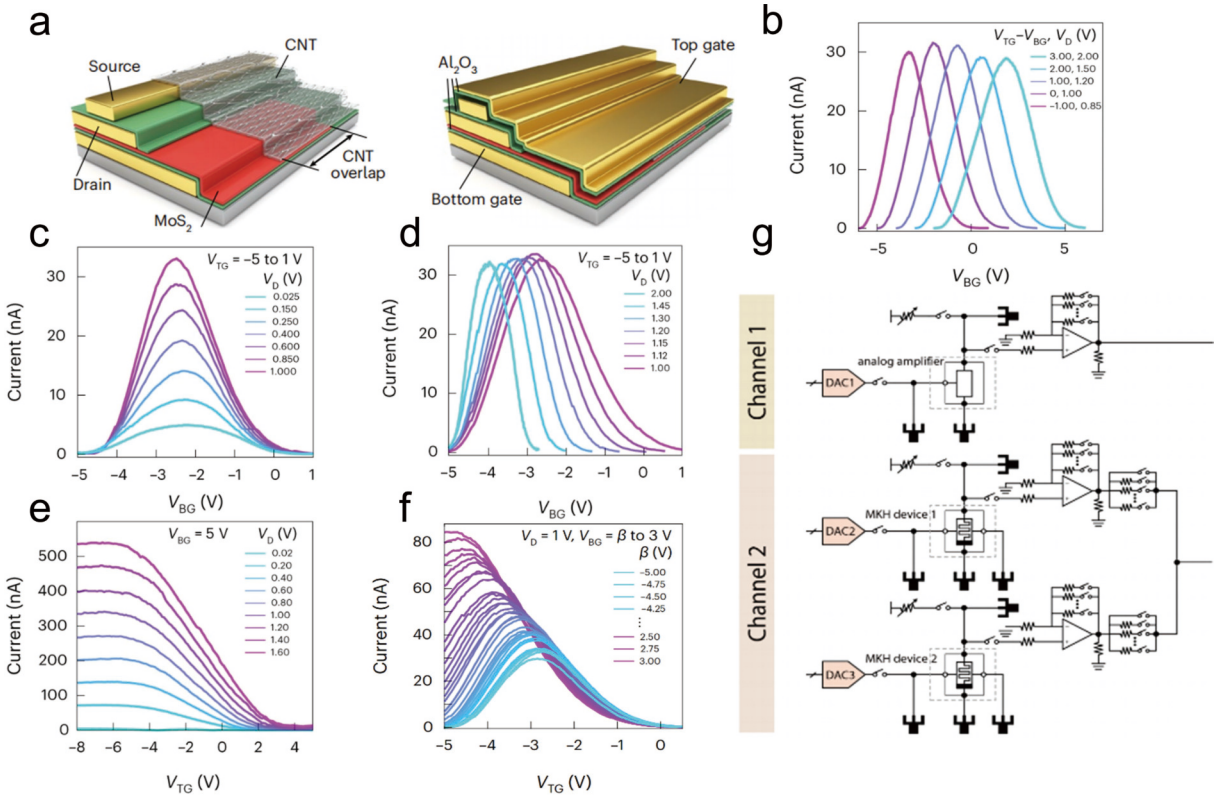

Fig. 9. (Color online) AI hardware implementations based on 2D reconfigurable mixed-kernel heterojunction (MKH) transistors. (a) The schematic of the MKH transistor based on MoS_2/CNT heterojunction. (b) The mean, (c) amplitude, and (d) standard deviation of the Gaussian function in I_D–V_{BG} curves can be individually controlled by the V_{TG}. (e) The tunable sigmoid function shown in the I_D–V_{TG} curves. (f) I_D–V_{TG} curves of the MKH transistor exhibit both Gaussian and sigmoid characteristics with a tunable mixing ratio under different bias configuration of V_{BG}. (g) The circuit of the hardware implementation of a mixed-kernel support vector machine classification for arrhythmia detection, which only consists two MKH transistors[99].

In addition to Gaussian functions, other kernel functions and mixed-kernel functions are also important in many AI algorithms, especially in SVMs that carry out classification and identification tasks. In 2023, a reconfigurable mixed-kernel heterojunction (MKH) transistor[99] was reported to generate reconfigurable Gaussian/sigmoid mixed-kernel function that can be controlled by the dual gates. Fig. 9(a) show the dual-gated and semi-vertical architecture of the MKH transistor based on 2D MoS_2/CNT heterojunction, which allows the dual gates controlling both the overlap and non-overlap regions of MoS_2 and CNT. Utilizing the weak electrostatic screening of the overlap region, the MKH transistor can generate Gaussian functions through sweeping the voltage of the back gate (V_{BG}), and the amplitude, mean and standard deviation of the Gaussian function can be individually controlled by the biasing configuration of the top gate (V_{TG}), which are shown respectively in Figs. 9(b)–9(d). Moreover, as shown in Fig. 9(e), the MKH transistor can also yield tunable sigmoid function by sweeping V_{TG} with a fixed V_{BG}, which was observed for the first time in anti-ambipolar devices. Therefore, tuning the bias condition of V_{BG} enables the I_D–V_{TG} curves of the MKH transistor exhibit both Gaussian and sigmoid characteristics with a tunable mixing ratio, as shown in Fig. 9(f). Additionally, the MKH transistors were used to demonstrate the hardware implementation of a mixed-kernel SVM classification for arrhythmia detection from ECG data, where the full circuit (Fig. 9(g)) consists only two MKH transistors. The mixed-kernel function generated by MKH transistors can significantly improve the personalized classification accuracy to about 90 %. It's worth noting that compared to traditional CMOS implementations that require at least 100 transistors, this MKH approach has outstanding advantages in reducing transistor usage, footprints and energy consumption, which is more significant in wearable applications and scalable implementations such as $n \times n$ kernel matrix.

Utilizing the charge effect at the interface of different 2D materials, by modulating the configurations of bias voltages, 2D reconfigurable devices can generate output characteristics with varying shapes and parameters to meet the requirements of different AI algorithms. In 2024, a multi-gate van der Waals interfacial junction transistor (vdW-IJT) based on a MoS_2/graphene heterostructure was reported to generate tunable Gaussian-like and π-shaped membership functions (MFs)[30]. As shown in Fig. 10(a), in the lateral junction of heavy n-doped (n^+) MoS_2 layer and p-doped graphene ribbon, the overlapping graphene region exhibits light n-type (n^-) doping due to the transporting of electron from MoS_2 to graphene. Therefore, the vdW-IJT has a lateral structure of $n^+/n^-/n^+$ homojunction in the MoS_2 channel, thus resulting in precise and effective control of doping level and carrier transport properties through the charge transfer effect at the interface. By applying different gate bias voltage configurations to the multi-gate vdW-IJT shown in Fig. 10(b), a single multi-gate vdW-IJT is able to generate π-shape and Gaussian-like shape I_{DS}–V_{G2} curves. When $V_{G1} < 1$ V, I_{DS} is mainly determined by V_{G2} as electrons can pass through G1. With the

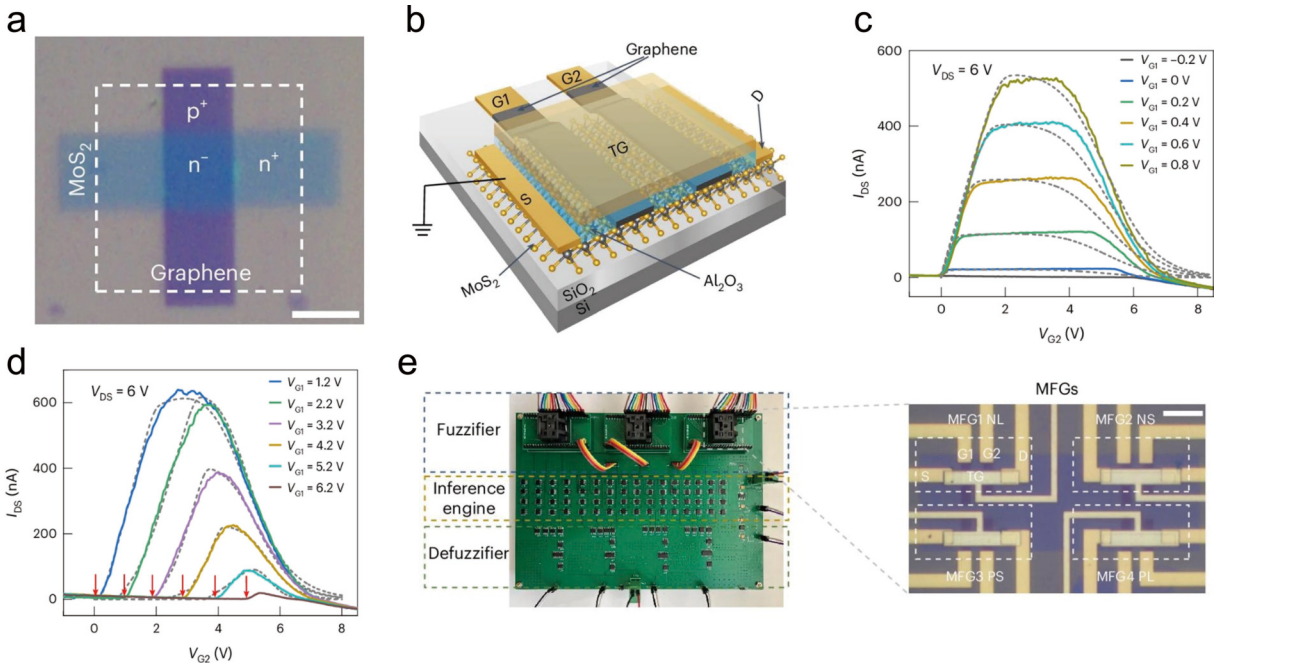

Fig. 10. (Color online) An FLS hardware based on the multi-gate van der Waals interfacial junction transistor (vdW-IJT). (a) Optical image of the lateral MoS_2/graphene junction. (b) Schematic of the multi-gate vdW-IJT with G1, G2, and a global top gate (TG). I_{DS}–V_{G2} curves of the multi-gate vdW-IJT showing (c) π-shape and (d) Gaussian-like shape membership functions. (e) The image of a complete FLS hardware on a PCB (left) and detailed image of four membership function generators in a chip (right) [30].

increase of V_{G2}, I_{DS} changes from being blocked to gradually increasing until saturation, and finally decreasing due to the recombination current becomes larger, thus resulting in the π-shape curves that can be modulated by V_{G1} as shown in Fig. 10(c). Similarly, if $V_{G1} > 1$ V, I_{DS} begins to increase from a certain voltage because V_{G2} must be large enough to prevent the electrons from leaking through G1, and I_{DS} begins to decrease due to the recombination current in G2, therefore the Gaussian-like shape curves was demonstrated in Fig. 10(d). Moreover, detailed parameters of these curves can be adjusted by V_{TG} and V_{DS}, which makes the vdW-IJT more suitable for applications.

Using the tunable Gaussian-like and π-shaped MFs, by being integrated with peripheral CMOS circuits, the multi-gate vdW-IJT can be used to create a fuzzy logic system (FLS) hardware, which can be operated as a fuzzy proportional–integral–derivative (PID) controller, as shown in Fig. 10(e). FLSs essentially represents a nonlinear mapping between the input space and the output space. The MFs generated by vdW-IJT not only effectively enhance the nonlinear mapping ability, but also make the PID controller more flexible and adaptable when interacting with humans, which resulting in a remarkable improvement in the performance of a fuzzy neural network (FNN) in image segmentation tasks. Moreover, other significant advantages of this vdW-IJT method include scalability and power cost.

3.3. 2D reconfigurable memristors for AI hardware implementations

In addition to specific functions, stochastic characteristics are also essential for many non-von-Neumann computing architectures including Boltzmann machines (BM). So far, memristors have been widely used to generate parameters and distributions with stochastic characteristics due to their various stochastic properties, which dependent on the random motions of the atoms and ions. In 2018, a horizontal MoS_2 memristor that is able to control the resistive state and thus showing memristive behaviors was reported, which is realized by the migration of defects in the MoS_2 film[106]. In addition to the defect migration[107–109], phase transitions in 2D materials can also result in memristive effects[110, 111]. Therefore, a large number of neuromorphic computing implementations have been explored based on different kinds of memristors, including artificial neural networks[104, 110, 112, 113], annealing systems[114], and true random number generators[115].

For example, a threshold-switching memristor (TSM) was constructed based on the vertical MoS_2/graphene vdWH in 2019[116]. Fig. 11(a) shows the schematic of the vertical MoS_2/graphene TSM, where the vertical structure allows the large-scale fabrication and high-density integration of the device[117]. This TSM device abruptly converts from high resistance state (HRS) to low resistance state (LRS) when the voltage of graphene electrode (V_{Gr}) increases to V_1. Similarly, the device abruptly reverts to HRS when V_{Gr} decreases below V_2. These nonvolatile switching characteristics of the threshold voltage are originating from the migration of oxygen ions in the MoS_2 layer, where the multiple grain boundaries (GBs) in the polycrystalline structure of the MoS_2 offer the migration channels.

Utilizing the switching characteristics, this TSM device was used to demonstrate an artificial neuron to reproduce the integration and refractory response of biological neurons. Fig. 11(b) shows the circuit diagram of the artificial neuron, which is consisted of one TSM device along with resistors and a capacitor (Co). Figs. 11(c) and 11(d) show the output spikes of the artificial neuron circuits that exhibiting integration and refractory period, respectively, where the input pulses have an amplitude of 8 V and a frequency of 5 kHz. These behaviors are generated by the threshold voltage

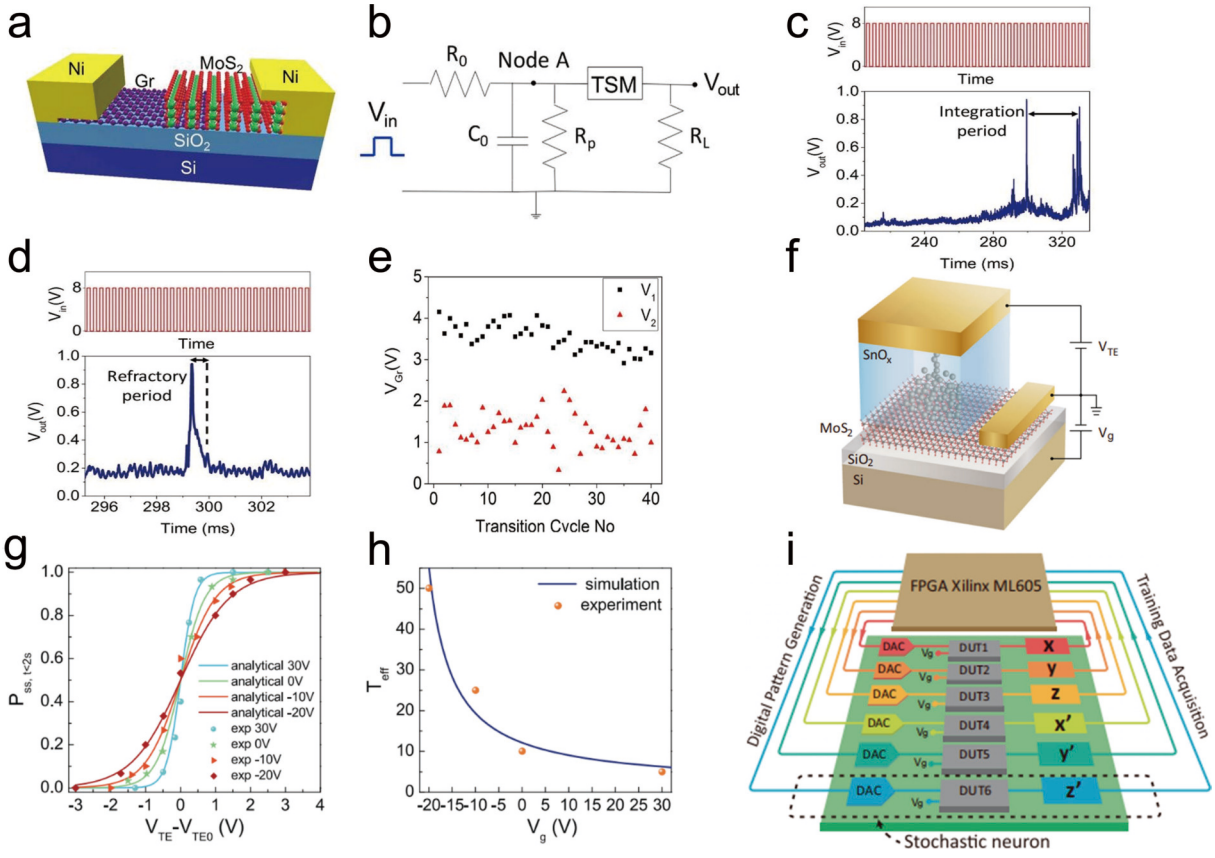

Fig. 11. (Color online) AI hardware implementations based on 2D reconfigurable memristors. (a) The schematic of the threshold-switching memristor based on the vertical MoS_2/graphene vdWH. (b) The circuit of the artificial neuron based on only one threshold-switching memristor. The output spikes of the artificial neuron circuit that exhibiting (c) integration period and (d) refractory period. (e) The stochastic distribution characteristics of V_1 and V_2 by repeating the switch of HRS/LRS[116]. (f) The schematic of the three-terminal stochastic memristor based on SnO_x/MoS_2 heterostructure. (g) The $P_{ss,t<2s}$– ($V_{TE} - V_{TE0}$) curves of the stochastic memristor show exponential-class sigmoidal distributions. (h) The relationship of the effective "temperature" (T_{eff}) and V_g. (i) The schematic of the Boltzmann machine circuit where each stochastic neuron consists only one stochastic memristor and a simple peripheral circuit[25].

switching of the TSM and the trapping/releasing of charge in Co. In addition, the frequency of spikes can be controlled by the amplitude of input pulses, which also mimics the characteristics of biological neurons. Furthermore, by repeating the switch of HRS/LRS for 40 times, we can observe the stochastic distribution characteristics of V_1 and V_2 as shown in Fig. 11(e), which are attributed to the stochastic nature from the motions of oxygen ions in MoS_2. These unique properties make the TSM device promising in neuromorphic sensors, hardware security and other real time computing applications.

However, the probability distributions of these memristors are not stable and cannot be precisely modulated, which limits their applications in the hardware implement of neural networks. To overcome these challenges, a three-terminal SnO_x/MoS_2 heterostructure memristor was reported to generate stochastic distributions with dynamically tunable parameters in 2021[25]. The architecture of the hetero-memristor is shown in Fig. 11(f), the amorphous SnO_x layer, which serves as the filament-switching layer, is sandwiched between the top electrode (TE) and the MoS_2 layer. Utilizing the stochastic characteristics in the filament-formation process that originating from the ionic random motion, this hetero-memristor can be used to demonstrate tunable statistical distributions from the set process, where the memristor is switched from high-resistance state to low-resistance due to the formation of the filament. By applying a V_{TE} to a high-resistance memristor, the probability that the memristor is successfully set within 2 s ($P_{ss,t<2s}$) shows exponential-class sigmoidal distributions in Fig. 11(g), where V_{TE0} refers to the V_{TE} point of 50% probability. Moreover, the $P_{ss,t<2s}$ curves also show that the gate bias (V_g) can modulate the 0–1 transition of the sigmoidal distributions, which is attributed to V_g tuning the electrical properties of MoS_2, thus controlling the potential distribution between SnO_x and MoS_2. Furthermore, the $P_{ss,t<2s}$ distribution can be approximated to a Fermi–Dirac like distribution $\left(P_{ss,t<2s} \approx \frac{1}{1+\exp\left(-\frac{V_{TE}-V_{TE0}}{T_{eff}}\right)}\right)$, where the effective "temperature" (T_{eff}) can be dynamically controlled by V_g (Fig. 11(h)).

Taking advantages of this hetero-memristor, a BM using simulated annealing based on reconfigurable stochastic neurons was demonstrated to solve a MAX-SAT problem. Each stochastic neuron consists only one memristor and a simple peripheral circuit, as shown in Fig. 11(i). More importantly, the tunable nature of the device allows the T_{eff} of the BM be dynamically tuned by V_g, thus enabling different "cooling" strategies of the BM, which avoids premature convergence and improves the accuracy of the BM, as well as reducing the usage of electronic elements and energy consumption.

4. Challenges and conclusion

Although a large number of studies have demonstrated the extraordinary advantages of 2D reconfigurable devices, there still lies several challenges in the growth of 2D materials and the fabrication process of these emerging devices.

First of all, in order to achieve the practical applications of 2D materials, having high-quality single crystalline wafer-scale 2D materials is of paramount importance. At present, since mechanical exfoliation method is not suitable for wafer-scale production, the best way to achieve wafer-scale 2D materials is bottom-up growing on the substrate. However, our current understanding of the growth and nucleation mechanisms of 2D materials under various conditions remains incomplete. This lack of comprehensive knowledge hinders the development of synthesis methods for wafer-scale 2D materials and brings significant challenges in controlling thickness, defects and lattice mismatch[118], while the method for manufacturing multilayer structures still awaits development. What's more, current seamless coalescence technology imposes strict requirements on the substrate processing[119].

In the fabrication process of 2D vdWHs, the lack in the methods of transfer and stacking 2D materials layers limits the large-scale integration of 2D reconfigurable devices[120], for example, wrinkles, defects, or cracks may occur on 2D material films while transferring devices. As a result, current 2D reconfigurable devices usually are faced with the issues of low device yield and high variability[121]. Moreover, influenced by the compatibility with silicon-based technology, leakage current and limited supply voltage, the performance of these devices also needs further improvement. To take the 2D reconfigurable devices into practical applications, the design complexity of the devices and corresponding circuits is another challenge apart from the limitations that have been mentioned above.

In this article, we began with introducing the limitations of traditional semiconductor technologies and reconfigurable circuits in improving integration density. Consequently, we introduced the outstanding characteristics of 2D materials and reconfigurable devices based on 2D materials that can realize reconfigurable functions at device level. To provide a review on the recent progress of emerging reconfigurable devices based on 2D materials and their related logic or analog applications, we introduced these devices from two perspectives: their functions at device level and their logic or analog application at circuit level. One notable feature of 2D reconfigurable devices is their ability to generate tunable anti-ambipolar characteristics, which are originated from the weak van der Waals interaction and effective control of transport conditions in 2D materials. We introduced the mechanism of typical AAT devices and summarized their applications in logic operations. Another significant function of 2D reconfigurable devices is demonstrating nonvolatile operations, which are achieved by the special design of floating gates and ferroelectric materials. We explained the working principles of several nonvolatile devices and introduced the devices that have nonvolatile multifunction and are used to realize logic-in-memory computing. As for the analog applications of AATs, we reviewed the analog signal frequency modulation circuits based on AATs. Furthermore, we introduced diverse AI hardware implementations that utilize reconfigurable transistors and memristors, highlighting the unique advantages of reconfigurable devices in the hardware applications. Finally, we discussed the challenges of current 2D reconfigurable devices and summarized the full article.

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References

[1] Loubet N, Hook T, Montanini P, et al. Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET. 2017 Symposium on VLSI Technology, 2017, T230

[2] Bravaix A, Hamparsoumian G, Sonzogni J, et al. CMOS scaling challenges for high performance and low power applications facing reliability criteria towards the decananometer range. J Phys: Conf Ser, 2023, 2548(1), 012003

[3] Radamson H H, He X B, Zhang Q Z, et al. Miniaturization of cmos. Micromachines, 2019, 10(5), 293

[4] Yin L, Cheng R Q, Wen Y, et al. Emerging 2D memory devices for in-memory computing. Adv Mater, 2021, 33(29), e2007081

[5] Lee H E, Park J H, Kim T J, et al. Novel electronics for flexible and neuromorphic computing. Adv Funct Materials, 2018, 28(32), 1801690

[6] Heinzig A, Pregl S, Trommer J, et al. Reconfigurable NAND-NOR circuits fabricated by a CMOS printing technique. 2017 IEEE 12th Nanotechnology Materials and Devices Conference (NMDC), 2017, 179

[7] Peng R X, Wu Y H, Wang B L, et al. Programmable graded doping for reconfigurable molybdenum ditelluride devices. Nat Electron, 2023, 6, 852

[8] Shingaya Y, Zulkefli A, Iwasaki T, et al. Dual-gate anti-ambipolar transistor with van der Waals ReS_2/WSe_2 heterojunction for reconfigurable logic operations. Adv Elect Materials, 2023, 9(1), 2200704

[9] Novoselov K S, Geim A K, Morozov S V, et al. Electric field effect in atomically thin carbon films. Science, 2004, 306(5696), 666

[10] Feng C Y, Wu W W, Liu H D, et al. Emerging opportunities for 2D materials in neuromorphic computing. Nanomaterials, 2023, 13(19), 2720

[11] Liu Y, Weiss N O, Duan X D, et al. Van der Waals heterostructures and devices. Nat Rev Mater, 2016, 1(9), 16042

[12] Lemme M C, Akinwande D, Huyghebaert C, et al. 2D materials for future heterogeneous electronics. Nat Commun, 2022, 13(1), 1392

[13] Liu C S, Chen H W, Wang S Y, et al. Two-dimensional materials for next-generation computing technologies. Nat Nanotechnol, 2020, 15(7), 545

[14] Lukman S, Ding L, Xu L, et al. High oscillator strength interlayer excitons in two-dimensional heterostructures for mid-infrared photodetection. Nat Nanotechnol, 2020, 15(8), 675

[15] Ye X L, Du Y N, Wang M Y, et al. Advances in the field of two-dimensional crystal-based photodetectors. Nanomaterials, 2023, 13(8), 1379

[16] Liu C Y, Guo J S, Yu L W, et al. Silicon/2D-material photodetectors: From near-infrared to mid-infrared. Light Sci Appl, 2021, 10(1), 123

[17] Liu Z J, Gong X G, Cheng J R, et al. Wafer-scale synthesis of two-

dimensional materials for integrated electronics. Chip, 2024, 3(1), 100080
[18] Zhang L N, Dong J C, Ding F. Strategies, status, and challenges in wafer scale single crystalline two-dimensional materials synthesis. Chem Rev, 2021, 121(11), 6321
[19] Chen T A, Chuu C P, Tseng C C, et al. Wafer-scale single-crystal hexagonal boron nitride monolayers on Cu (111). Nature, 2020, 579(7798), 219
[20] Yang P F, Zhang S Q, Pan S Y, et al. Epitaxial growth of centimeter-scale single-crystal MoS_2 monolayer on Au(111). ACS Nano, 2020, 14(4), 5036
[21] Fei W W, Trommer J, Lemme M C, et al. Emerging reconfigurable electronic devices based on two-dimensional materials: A review. InfoMat, 2022, 4(10), e12355
[22] Mir S H, Yadav V K, Singh J K. Recent advances in the carrier mobility of two-dimensional materials: A theoretical perspective. ACS Omega, 2020, 5(24), 14203
[23] Gomes F O V, Pokle A, Marinkovic M, et al. High mobility solution processed MoS_2 thin film transistors. Solid State Electron, 2019, 158, 75
[24] Cao W, Chu J H, Parto K, et al. A mode-balanced reconfigurable logic gate built in a van der Waals strata. NPJ 2D Mater Appl, 2021, 5, 20
[25] Yan X D, Ma J H, Wu T, et al. Reconfigurable Stochastic neurons based on tin oxide/MoS_2 hetero-memristors for simulated annealing and the Boltzmann machine. Nat Commun, 2021, 12, 5710
[26] Chaves A, Azadani J G, Alsalman H, et al. Bandgap engineering of two-dimensional semiconductor materials. NPJ 2D Mater Appl, 2020, 4, 29
[27] Jung D Y, Yang S Y, Park H, et al. Interface engineering for high performance graphene electronic devices. Nano Convergence, 2015, 2(1), 11
[28] Sangwan V K, Beck M E, Henning A, et al. Self-aligned van der Waals heterojunction diodes and transistors. Nano Lett, 2018, 18(2), 1421
[29] Xiong X, Kang J Y, Hu Q L, et al. Reconfigurable logic-in-memory and multilingual artificial synapses based on 2D heterostructures. Adv Funct Materials, 2020, 30(11), 1909645
[30] Liu H F, Wu J B, Ma J H, et al. A van der Waals interfacial junction transistor for reconfigurable fuzzy logic hardware. Nat Electron, 2024, 7, 876
[31] Beck M E, Shylendra A, Sangwan V K, et al. Spiking neurons from tunable Gaussian heterojunction transistors. Nat Commun, 2020, 11(1), 1565
[32] Meng Y, Wang W, Wang W, et al. Anti-ambipolar heterojunctions: Materials, devices, and circuits. Adv Mater, 2024, 36(17), e2306290
[33] Chhowalla M, Jena D, Zhang H. Two-dimensional semiconductors for transistors. Nat Rev Mater, 2016, 1(11), 16052
[34] Li H, Ling J Y, Lin J M, et al. Interface engineering in two-dimensional heterostructures towards novel emitters. J Semicond, 2023, 44(1), 011001
[35] Wang H Y, Song X Y, Li Z X, et al. Recent advances in two-dimensional photovoltaic devices. J Semicond, 2024, 45(5), 051701
[36] Thakar K, Lodha S. Multi-bit analog transmission enabled by electrostatically reconfigurable ambipolar and anti-ambipolar transport. ACS Nano, 2021, 15(12), 19692
[37] Jariwala D, Sangwan V K, Wu C C, et al. Gate-tunable carbon nanotube-MoS_2 heterojunction p-n diode. Proc Natl Acad Sci USA, 2013, 110(45), 18076
[38] Nourbakhsh A, Zubair A, Dresselhaus M S, et al. Transport properties of a MoS_2/WSe_2 heterojunction transistor and its potential for application. Nano Lett, 2016, 16(2), 1359
[39] Roy T, Tosun M, Cao X, et al. Dual-gated MoS_2/WSe_2 van der Waals tunnel diodes and transistors. ACS Nano, 2015, 9(2), 2071
[40] Huo N J, Yang J H, Huang L, et al. Tunable polarity behavior and self-driven photoswitching in p-WSe_2/n-WS_2 heterojunctions. Small, 2015, 11(40), 5430
[41] Huang M Q, Li S M, Zhang Z F, et al. Multifunctional high-performance van der Waals heterostructures. Nat Nanotechnol, 2017, 12(12), 1148
[42] Li Y T, Wang Y, Huang L, et al. Anti-ambipolar field-effect transistors based on few-layer 2D transition metal dichalcogenides. ACS Appl Mater Interfaces, 2016, 8(24), 15574
[43] Yan R S, Fathipour S, Han Y M, et al. Esaki diodes in van der Waals heterojunctions with broken-gap energy band alignment. Nano Lett, 2015, 15(9), 5791
[44] Hayakawa R, Takahashi K, Zhong X H, et al. Reconfigurable logic-in-memory constructed using an organic antiambipolar transistor. Nano Lett, 2023, 23(17), 8339
[45] Kobashi K, Hayakawa R, Chikyow T, et al. Multi-valued logic circuits based on organic anti-ambipolar transistors. Nano Lett, 2018, 18(7), 4355
[46] Shim J, Oh S, Kang D H, et al. Phosphorene/rhenium disulfide heterojunction-based negative differential resistance device for multi-valued logic. Nat Commun, 2016, 7, 13413
[47] Maeda K, Okabayashi N, Kano S, et al. Logic operations of chemically assembled single-electron transistor. ACS Nano, 2012, 6(3), 2798
[48] Wakayama Y, Hayakawa R. Antiambipolar transistor: A newcomer for future flexible electronics. Adv Funct Materials, 2020, 30(20), 1903724
[49] Yoo H, Kim C H. Multi-valued logic system: New opportunities from emerging materials and devices. J Mater Chem C, 2021, 9(12), 4092
[50] Kim C H, Hayakawa R, Wakayama Y. Fundamentals of organic anti-ambipolar ternary inverters. Adv Elect Materials, 2020, 6(3), 1901200
[51] Kim J B, Li J S, Choi Y, et al. Photosensitive graphene P-N junction transistors and ternary inverters. ACS Appl Mater Interfaces, 2018, 10(15), 12897
[52] Wu E X, Xie Y, Liu Q Z, et al. Photoinduced doping to enable tunable and high-performance anti-ambipolar $MoTe_2/MoS_2$ heterotransistors. ACS Nano, 2019, 13(5), 5430
[53] Lim J H, Shim J, Kang B S, et al. Double negative differential transconductance characteristic: From device to circuit application toward quaternary inverter. Adv Funct Materials, 2019, 29(48), 1905540
[54] Jung K S, Heo K, Kim M J, et al. Double negative differential resistance device based on hafnium disulfide/pentacene hybrid structure. Adv Sci, 2020, 7(19), 2000991
[55] Kim K H, Park H Y, Shim J, et al. A multiple negative differential resistance heterojunction device and its circuit application to ternary static random access memory. Nanoscale Horiz, 2020, 5(4), 654
[56] Yang B H, Chen J, Tu F B. Towards efficient generative AI and beyond-AI computing: New trends on ISSCC 2024 machine learning accelerators. J Semicond, 2024, 45(4), 040204
[57] Zou X Q, Xu S, Chen X M, et al. Breaking the von Neumann bottleneck: Architecture-level processing-in-memory technology. Sci China Inf Sci, 2021, 64(6), 160404
[58] Sasaki T, Ueno K, Taniguchi T, et al. Material and device structure designs for 2D memory devices based on the floating gate voltage trajectory. ACS Nano, 2021, 15(4), 6658
[59] Bertolazzi S, Bondavalli P, Roche S, et al. Nonvolatile memories

based on graphene and related 2D materials. Adv Mater, 2019, 31(10), e1806663

[60] Seo S, Lee J J, Lee H J, et al. Recent progress in artificial synapses based on two-dimensional van der Waals materials for brain-inspired computing. ACS Appl Electron Mater, 2020, 2(2), 371

[61] Li D, Chen M Y, Sun Z Z, et al. Two-dimensional non-volatile programmable p-n junctions. Nat Nanotechnol, 2017, 12(9), 901

[62] Yin L, Wang F, Cheng R Q, et al. Van der Waals heterostructure devices with dynamically controlled conduction polarity and multifunctionality. Adv Funct Materials, 2019, 29(1), 1804897

[63] Xiong X, Kang J Y, Liu S Y, et al. Nonvolatile logic and ternary content-addressable memory based on complementary black phosphorus and rhenium disulfide transistors. Adv Mater, 2022, 34(48), e2106321

[64] Kumar A, Giubileo F, Sleziona S, et al. Temperature dependent black phosphorus transistor and memory. Nano Ex, 2023, 4(1), 014001

[65] Liu L, Liu C S, Jiang L L, et al. Ultrafast non-volatile flash memory based on van der Waals heterostructures. Nat Nanotechnol, 2021, 16(8), 874

[66] Hou X, Yan X, Liu C S, et al. Operation mode switchable charge-trap memory based on few-layer MoS_2. Semicond Sci Technol, 2018, 33(3), 034001

[67] Zhang E Z, Wang W Y, Zhang C, et al. Tunable charge-trap memory based on few-layer MoS_2. ACS Nano, 2015, 9(1), 612

[68] Zhang P F, Li D, Chen M Y, et al. Floating-gate controlled programmable non-volatile black phosphorus PNP junction memory. Nanoscale, 2018, 10(7), 3148

[69] Vu Q A, Shin Y S, Kim Y R, et al. Two-terminal floating-gate memory with van der Waals heterostructures for ultrahigh on/off ratio. Nat Commun, 2016, 7, 12725

[70] Luo Z D, Zhang S Q, Liu Y, et al. Dual-ferroelectric-coupling-engineered two-dimensional transistors for multifunctional in-memory computing. ACS Nano, 2022, 16(2), 3362

[71] Sheng Z, Dong J G, Hu W N, et al. Reconfigurable logic-in-memory computing based on a polarity-controllable two-dimensional transistor. Nano Lett, 2023, 23(11), 5242

[72] Sun X X, Zhu C G, Yi J L, et al. Reconfigurable logic-in-memory architectures based on a two-dimensional van der Waals heterostructure device. Nat Electron, 2022, 5, 752

[73] Zhao Z J, Rakheja S, Zhu W J. Nonvolatile reconfigurable 2D Schottky barrier transistors. Nano Lett, 2021, 21(21), 9318

[74] Seo S Y, Moon G, Okello O F N, et al. Reconfigurable photo-induced doping of two-dimensional van der Waals semiconductors using different photon energies. Nat Electron, 2021, 4, 38

[75] Migliato Marega G, Zhao Y F, Avsar A, et al. Logic-in-memory based on an atomically thin semiconductor. Nature, 2020, 587(7832), 72

[76] Hou X, Liu C S, Ding Y, et al. A logic-memory transistor with the integration of visible information sensing-memory-processing. Adv Sci, 2020, 7(21), 2002072

[77] Cheng R Q, Wang F, Yin L, et al. High-performance, multifunctional devices based on asymmetric van der Waals heterostructures. Nat Electron, 2018, 1, 356

[78] Yap W C, Jiang H, Liu J L, et al. Ferroelectric transistors with monolayer molybdenum disulfide and ultra-thin aluminum-doped hafnium oxide. Appl Phys Lett , 2017, 111(1), 013103

[79] Shekhawat A, Walters G, Yang N, et al. Data retention and low voltage operation of $Al_2O_3/Hf_{0.5}Zr_{0.5}O_2$ based ferroelectric tunnel junctions. Nanotechnology, 2020, 31(39), 39LT01

[80] Zhao R T, Zhao X Y, Liu H F, et al. Reconfigurable logic-memory hybrid device based on ferroelectric $Hf_{0.5}Zr_{0.5}O_2$. IEEE Electron Device Lett, 2021, 42(8), 1164

[81] Lv L, Zhuge F W, Xie F J, et al. Reconfigurable two-dimensional optoelectronic devices enabled by local ferroelectric polarization. Nat Commun, 2019, 10(1), 3331

[82] Zhu C C, Wang Y R, Wang F, et al. Nonvolatile reconfigurable broadband photodiodes based on BP/α-In_2Se_3 ferroelectric p–n junctions. Appl Phys Lett, 2022, 120(8), 083101

[83] Chen L, Wang T Y, Dai Y W, et al. Ultra-low power $Hf_{0.5}Zr_{0.5}O_2$ based ferroelectric tunnel junction synapses for hardware neural network applications. Nanoscale, 2018, 10(33), 15826

[84] Wang Y R, Wang F, Wang Z X, et al. Reconfigurable photovoltaic effect for optoelectronic artificial synapse based on ferroelectric p-n junction. Nano Res, 2021, 14(11), 4328

[85] Tsai M Y, Huang C T, Lin C Y, et al. A reconfigurable transistor and memory based on a two-dimensional heterostructure and photoinduced trapping. Nat Electron, 2023, 6, 755

[86] Bae J H, Kim H, Kwon D, et al. Reconfigurable field-effect transistor as a synaptic device for XNOR binary neural network. IEEE Electron Device Lett, 2019, 40(4), 624

[87] Yin L, Cheng R Q, Wang Z X, et al. Two-dimensional unipolar memristors with logic and memory functions. Nano Lett, 2020, 20(6), 4144

[88] Liu C S, Chen H W, Hou X, et al. Small footprint transistor architecture for photoswitching logic and *in situ* memory. Nat Nanotechnol, 2019, 14(7), 662

[89] Liu C S, Yan X, Song X F, et al. A semi-floating gate memory based on van der Waals heterostructures for quasi-non-volatile applications. Nat Nanotechnol, 2018, 13(5), 404

[90] Li J Y, Zhang H, Ding Y, et al. A non-volatile AND gate based on $Al_2O_3/HfO_2/Al_2O_3$ charge-trap stack for *in situ* storage applications. Sci Bull, 2019, 64(20), 1518

[91] Zhang X H, Peng B. The twisted two-dimensional ferroelectrics. J Semicond, 2023, 44(1), 011002

[92] Yao H, Wu E X, Liu J. Frequency doubler based on a single $MoTe_2/MoS_2$ anti-ambipolar heterostructure. Appl Phys Lett, 2020, 117(12), 1231, 03

[93] Lee M, Kim T W, Park C Y, et al. Graphene bridge heterostructure devices for negative differential transconductance circuit applications. Nanomicro Lett, 2022, 15(1), 22

[94] Yuce M R, Liu W T. A low-power multirate differential PSK receiver for space applications. IEEE Trans Veh Technol, 2005, 54(6), 2074

[95] Das S, Das S. Digital keying enabled by reconfigurable 2D modulators. Adv Mater, 2022, 34(43), e2203753

[96] Jariwala D, Sangwan V K, Seo J T, et al. Large-area, low-voltage, antiambipolar heterojunctions from solution-processed semiconductors. Nano Lett, 2015, 15(1), 416

[97] Crespo J L, Duro R J, Pena F L. Gaussian synapse ANNs in multi- and hyperspectral image data analysis. IEEE Trans Instrum Meas, 2003, 52(3), 724

[98] Sebastian A, Pannone A, Subbulakshmi Radhakrishnan S, et al. Gaussian synapses for probabilistic neural networks. Nat Commun, 2019, 10(1), 4199

[99] Yan X D, Qian J H, Ma J H, et al. Reconfigurable mixed-kernel heterojunction transistors for personalized support vector machine classification. Nat Electron, 2023, 6, 862

[100] Sangwan V K, Hersam M C. Neuromorphic nanoelectronic materials. Nat Nanotechnol, 2020, 15(7), 517

[101] Maass W. Networks of spiking neurons: The third generation of neural network models. Neural Netw, 1997, 10(9), 1659

[102] Gao L G, Chen P Y, Yu S M. NbO_x based oscillation neuron for neuromorphic computing. Appl Phys Lett, 2017, 111(10), 103503

[103] Wang J Y, Teng C J, Zhang Z Y, et al. A scalable artificial neuron based on ultrathin two-dimensional titanium oxide. ACS Nano, 2021, 15(9), 15123
[104] Wang Z R, Joshi S, Savel'ev S, et al. Fully memristive neural networks for pattern classification with unsupervised learning. Nat Electron, 2018, 1, 137
[105] Wang Z, Crafton B, Gomez J, et al. Experimental demonstration of ferroelectric spiking neurons for unsupervised clustering. 2018 IEEE International Electron Devices Meeting (IEDM), 2018, 13.3.1
[106] Sangwan V K, Jariwala D, Kim I S, et al. Gate-tunable memristive phenomena mediated by grain boundaries in single-layer MoS_2. Nat Nanotechnol, 2015, 10(5), 403
[107] Wang M, Cai S H, Pan C, et al. Robust memristors based on layered two-dimensional materials. Nat Electron, 2018, 1, 130
[108] Shi Y Y, Liang X H, Yuan B, et al. Electronic synapses made of layered two-dimensional materials. Nat Electron, 2018, 1, 458
[109] Sun L F, Hwang G, Choi W, et al. Ultralow switching voltage slope based on two-dimensional materials for integrated memory and neuromorphic applications. Nano Energy, 2020, 69, 104472
[110] Zhu X J, Li D, Liang X G, et al. Ionic modulation and ionic coupling effects in MoS_2 devices for neuromorphic computing. Nat Mater, 2019, 18(2), 141
[111] Zhang F, Zhang H R, Krylyuk S, et al. Electric-field induced structural transition in vertical $MoTe_2$- and $Mo_{1-x}W_xTe_2$-based resistive memories. Nat Mater, 2019, 18(1), 55
[112] Feng X W, Li Y D, Wang L, et al. A fully printed flexible MoS_2 memristive artificial synapse with femtojoule switching energy. Adv Elect Mater, 2019, 5(12), 1900740
[113] Wang K Y, Li L T, Zhao R J, et al. A pure 2H-MoS_2 nanosheet-based memristor with low power consumption and linear multilevel storage for artificial synapse emulator. Adv Elect Mater, 2020, 6(3), 1901342
[114] Cai F X, Kumar S, Van Vaerenbergh T, et al. Power-efficient combinatorial optimization using intrinsic noise in memristor Hopfield neural networks. Nat Electron, 2020, 3, 409
[115] Jiang H, Belkin D, Savel'ev S E, et al. A novel true random number generator based on a stochastic diffusive memristor. Nat Commun, 2017, 8(1), 882
[116] Kalita H, Krishnaprasad A, Choudhary N, et al. Artificial neuron using vertical MoS_2/graphene threshold switching memristors. Sci Rep, 2019, 9(1), 53
[117] Bez R, Camerlenghi E, Modelli A, et al. Introduction to flash memory. Proc IEEE, 2003, 91(4), 489
[118] Wang D, Zhang Z C, Li B, et al. Synthesis of two-dimensional/one-dimensional heterostructures with tunable width. J Semicond, 2021, 42(9), 092001
[119] Zhao T G, Guo J X, Li T T, et al. Substrate engineering for wafer-scale two-dimensional material growth: Strategies, mechanisms, and perspectives. Chem Soc Rev, 2023, 52(5), 1650
[120] Quellmalz A, Wang X J, Sawallich S, et al. Large-area integration of two-dimensional materials and their heterostructures by wafer bonding. Nat Commun, 2021, 12(1), 917
[121] Chen S C, Mahmoodi M R, Shi Y Y, et al. Wafer-scale integration of two-dimensional materials in high-density memristive crossbar arrays for artificial neural networks. Nat Electron, 2020, 3, 638

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