Journal of Semiconductors, 2025, 46, 110401
DOI: 10.1088/1674-4926/25080028
CSTR: 32376.14.1674-4926.25080028

NEWS AND VIEWS

Contact planarization and passivation lift tungsten diselenide PMOS performance

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Citation: H Y Peng, P H Tan, and J B Wu, Contact planarization and passivation lift tungsten diselenide PMOS performance[J]. *J. Semicond.*, 2025, 46(11), 110401. https://doi.org/10.1088/1674-4926/25080028

Two-dimensional (2D) transition metal dichalcogenides (TMDs), which allow atomic-scale manipulation, have superior electrical and optical properties that challenge the limits of traditional bulk semiconductors like silicon[1, 2]. As a representative TMD and a promising 2D channel material for high-performance, scalable p-type transistors, tungsten diselenide (WSe_2) has attracted considerable academic and industrial interest for its potential in advanced complementary metal–oxide–semiconductor (CMOS) logic technology and in extending Moore's Law[3−7]. After years of research and development, the basic properties of WSe_2 are now well understood[3−7]. However, compared to n-type TMDs such as molybdenum disulfide (MoS_2)—where researchers have achieved low-resistance contacts[8, 9] and high carrier mobilities[10]—WSe_2 still lags behind. WSe_2 device performance has been limited by strong Fermi-level pinning at the contacts, poor interface quality, and unstable device behavior. These factors lead to high contact resistance (R_c), resulting in high threshold voltages (V_{th}), suboptimal subthreshold swings (SS), and significant hysteresis. Recently, two groundbreaking studies presented at the 2025 VLSI Symposium unveiled pathways to overcome these hurdles, demonstrating record performance in WSe_2 p-channel transistors through innovative engineering. Each study tackles the problem from different angles—including surface conditioning, contact engineering, gate oxide scaling, and passivation—and each achieves significant performance improvements in monolayer and multilayer WSe_2 transistors. In this "NEWS AND VIEWS" article, we briefly highlight their key ideas and results.

In the first study[11], researchers at TSMC made monolayer WSe_2 more competitive as a scaled p-channel transistor candidate. They grew monolayer WSe_2 by chemical vapor deposition (CVD) on sapphire wafers and mechanically transferred it onto target substrates with sealed dielectrics and metal gates, yielding hundreds of back-gated field-effect transistors (FETs) of various channel lengths and widths for characterization. The team addressed performance constraints in four key areas. First, they improved surface preparation and passivation before and after transferring the 2D channel. During transfer, a substrate pretreatment rendered the dielectric surface hydrophilic, and a post-transfer cleaning removed residues after channel transfer and active-area patterning. These steps reduced process residues and improved device uniformity (Fig. 1(a)). As a result, the drain current increased by about two orders of magnitude, the threshold voltage remained around −1.4 to −1.3 V, and the SS dropped to 200 mV/dec. Second, the TSMC team introduced contact engineering to mitigate Fermi-level pinning and metal-induced gap states. Beam lithography used for defining contacts can induce defects in WSe_2. To counter this, the researchers added a sacrificial contact buffer (SCB) layer on WSe_2 to absorb damage from particle bombardment, thereby reducing defect formation. They also inserted a thin contact liner to alleviate Fermi-level pinning from high-work-function metals (Ni, Pd, Pt) by preventing excessive orbital coupling at the metal-WSe_2 interface. These interface engineering steps improved the drain current (I_d) to over 10 A/m and reduced SS to below 200 mV/dec (Fig. 1(b)). Third, they scaled down the gate dielectric thickness (effective oxide thickness, EOT) to boost electrostatic control. Using a thinner HfO_x dielectric (4 nm physical thickness), the devices achieved steeper subthreshold slopes, improving SS from about 180 mV/dec to about 120 mV/dec (Fig. 1(c)). Finally, post-fabrication treatments were applied to enhance performance and stability. After device fabrication, a free-radical treatment followed by passivation significantly improved overall performance—reducing hysteresis and preserving stability even after one week of air exposure. With these holistic optimizations, the CVD-grown monolayer WSe_2 p-FETs achieved higher drive currents with reduced hysteresis, and they operate as normally-off devices within a reasonable voltage range (Fig. 1(d)).

A complementary study by researchers at Intel Corporation[12] tackled the contact problem using a manufacturable physical vapor deposition (PVD) sputtering process. This approach to forming contacts in back-gated WSe_2 transistors is compatible with high-volume manufacturing and competitive with lab-scale techniques like evaporation and atomic layer deposition (ALD) (Fig. 2(a)). The Intel team performed a systematic exploration of sputtered contacts on multilayer WSe_2 grown by metal–organic chemical vapor deposition (MOCVD). Using a bilayer resist stack for source/drain patterning and sputter deposition, they achieved an effective channel length of 190 nm due to controlled deposition into the resist undercut (Fig. 2(b)). Multiple process variables were examined to optimize the sputtered contacts, including adding an antimony (Sb) interlayer during platinum deposition, post-deposition annealing at various temperatures, con-

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Received 23 AUGUST 2025.

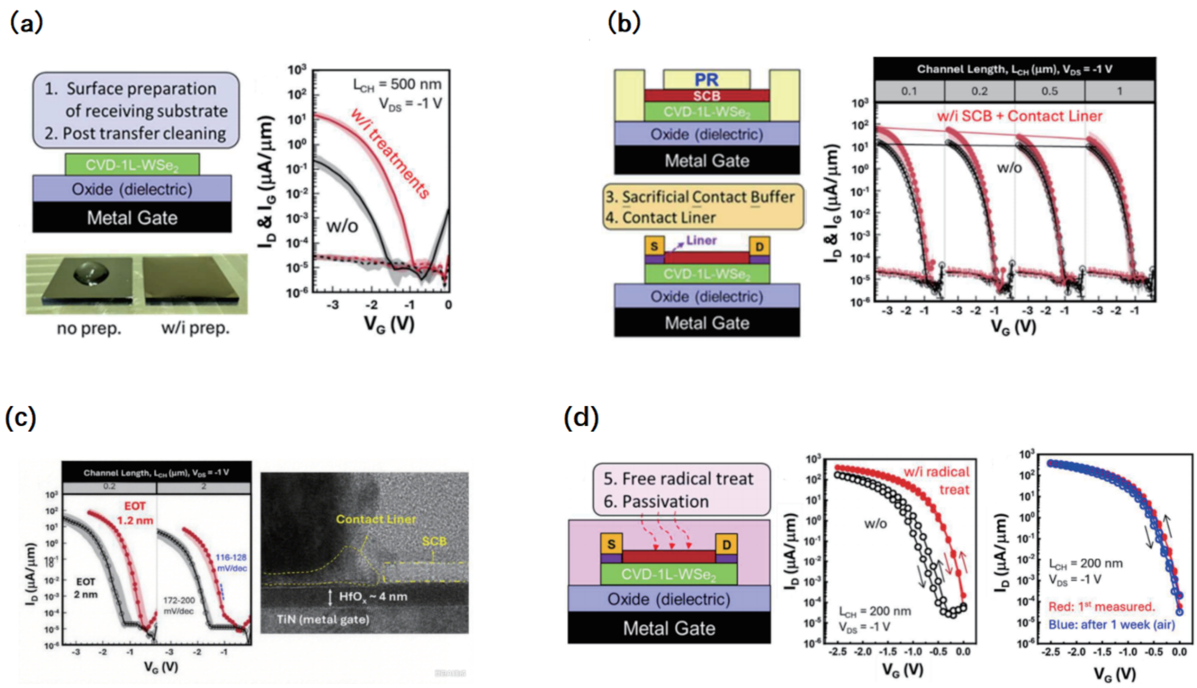

Fig. 1. (Color online) (a) Diagram illustrating key steps in the WSe_2 transfer process, along with photographs of samples with different surface treatments, and the resulting transfer characteristics of WSe_2 p-FETs. (b) Process flow for reducing beam-induced damage in the contact region, and transfer characteristics of WSe_2 p-FETs with and without an SCB layer and contact liner. (c)Transfer characteristics of WSe_2 p-FETs with a scaled gate dielectric (4 nm HfO_x alongside a high-resolution cross-sectional TEM image of the device structure. (d)Key steps in post-fabrication channel treatments, showing transfer curves of WSe_2 p-FETs with and without a free-radical treatment, and a comparison of device performance before and after one week of ambient aging[11].

tact metal thickness, and alternative metals. Under optimized conditions—for example, annealing at 180 °C for 10 min—device performance improved significantly (Fig. 2(c)). However, further annealing at 250 °C produced only a slight positive shift in threshold voltage, likely due to oxidation of the exposed channel. The investigation was extended to transistors with a gate-all-around (GAA) architecture. The researchers developed a new integration flow that utilizes contact planarization via chemical–mechanical polishing (CMP) for monolayer WSe_2 GAA FETs (Fig. 2(d)). Using this approach, they demonstrated devices with a SS of 132 mV/dec and a maximum drain current $I_{d,max}$ of 613 μA/μm (highlighted in Fig. 2(e))—nearly an order of magnitude higher drive current than prior WSe_2 devices with evaporated contacts. Clearly, sputtering provides a robust path to explore a wide range of contact materials, greatly improving 2D p-FET performance in both global back-gate and GAA configurations.

Two studies at the 2025 VLSI Symposium map a practical path for WSe_2 PMOS. The TSMC work cleans and passivates interfaces during and after transfer, adds an SCB and a thin liner at the contacts to ease Fermi level pinning, scales EOT with HfO_x for stronger gate control, and applies a post process free radical treatment that cuts hysteresis and improves air stability. The Intel work uses PVD sputtered contacts that are compatible with BEOL flows, tunes metal choice and anneal windows on multilayer WSe_2, and planarizes contacts with CMP for GAA devices. Reported figures include SS = 132 mV/dec and $I_{d,max}$ = 613 μA/μm. The message is clear. Interfaces and contacts set the ceiling and coordinated engineering lifts it.

Next steps should target three fronts. Variability and reliability need across wafer statistics and aging data under bias and temperature with a focus on interface traps and hysteresis drift. A stable process window should balance sputter energy and lattice damage, set SCB thickness and chemistry, match metal work function and channel electrostatics, and stay BEOL compatible. Circuit proof at low supply voltage should include inverter chains and ring oscillators with basic yield and tolerance models. Promising directions include orientation and strain control for better hole injection, controlled epitaxy for layer number and domains, *in situ* growth and *in situ* dielectric deposition to avoid transfer contamination, careful tuning of work function and interface dipoles, and robust Al_2O_3/HfO_x gate stacks. Scaling from single FETs to millimetre scale arrays with statistics will turn strong devices into reliable technology.

References

[1] Chen J, Sun M Y, Wang Z H, et al. Performance limits and advancements in single 2D transition metal dichalcogenide transistor. Nanomicro Lett, 2024, 16(1), 264

[2] Wu R X, Tao Q Y, Li J, et al. Bilayer tungsten diselenide transistors with on-state currents exceeding 1.5 milliamperes per micrometre. Nat Electron, 2022, 5(8), 497

[3] Park J H, Fathipour S, Kwak I, et al. Atomic layer deposition of Al_2O_3 on WSe_2 functionalized by titanyl phthalocyanine. ACS Nano, 2016, 10(7), 6888

[4] Wang Y, Chhowalla M. Making clean electrical contacts on 2D transition metal dichalcogenides. Nat Rev Phys, 2022, 4, 101

[5] Han H C, Zhang B Q, Zhang Z H, et al. Light-triggered anti-ambipolar transistor based on an in-plane lateral homojunction. Nano Lett, 2024, 24(28), 8602

[6] Lin Y T, Hsu C H, Chou A S, et al. Antimony-platinum modulated

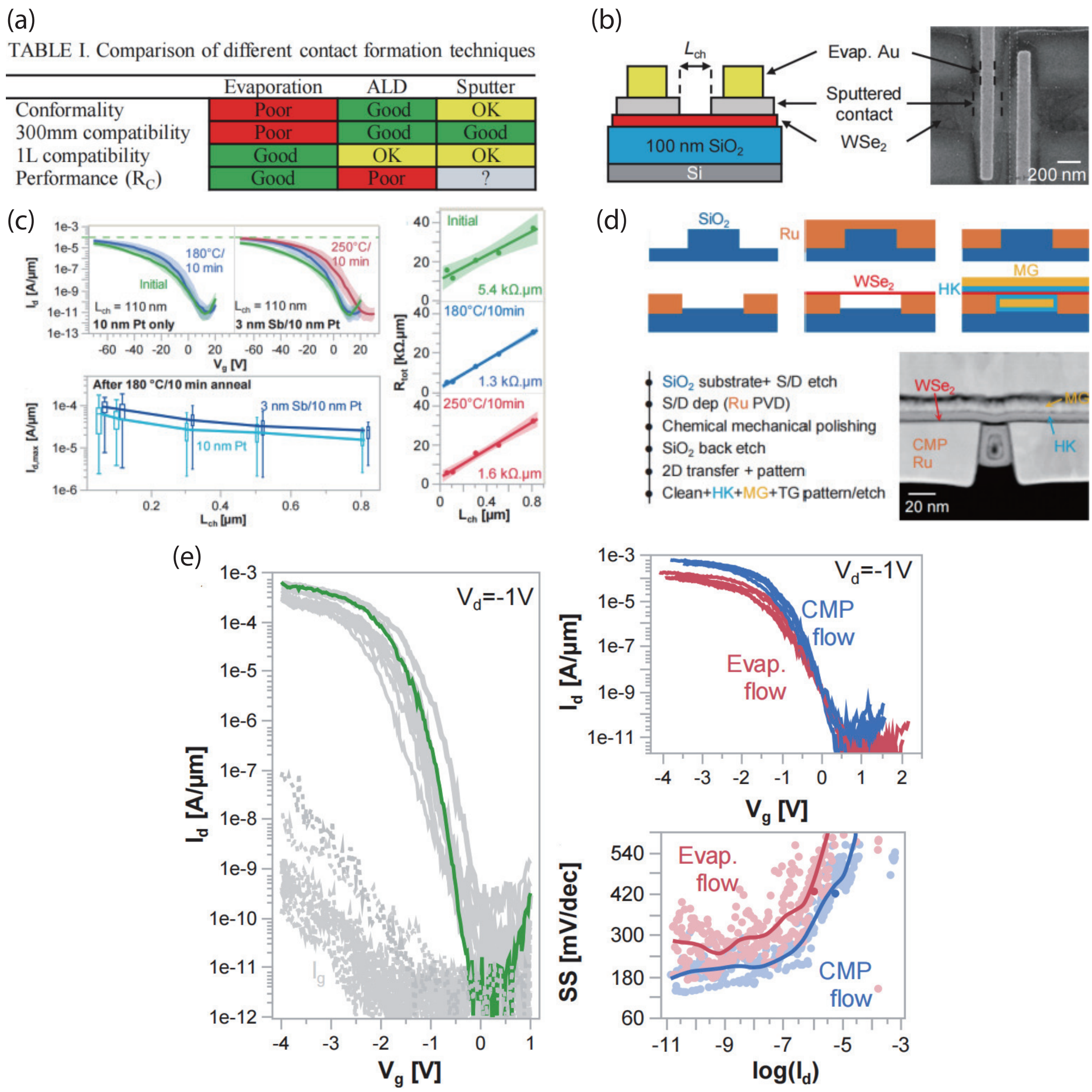

Fig. 2. (Color online) (a) Comparison of techniques (evaporation, ALD, sputtering) for forming contacts to TMD transistors. (b) Cross-sectional schematic of a back-end-of-line (BEOL) compatible back-gated multilayer WSe_2 transistor, alongside an SEM image of the fabricated device. (c) Transfer curves (I_d–V_g) for devices with L_{ch} = 110 nm, comparing Pt-only and Sb/Pt contacts at V_d = −1 V under different annealing conditions. Also shown is total resistance (R_{tot}) vs. channel length (10th percentile) extracted at V_d = −50 mV with $N_{inv} \approx 1 \times 10^{13}$ cm^{-2}. (d) Process flow for a monolayer WSe_2 GAA FET, featuring CMP-planarized PVD Ru source/drain contacts, and a cross-sectional TEM image of a GAA WSe_2 transistor with L_{sd} = 20 nm. (e) Measured I_d–V_g curves for devices with L_{sd} from 20 to 80 nm, highlighting the record SS = 132 mV/dec and $I_{d,max}$ of 613 μA/μm. Also shown are comparisons of transfer characteristics and SS for GAA WSe_2 FETs using CMP-formed Ru contacts versus evaporated Ru contacts[12].

contact enabling majority carrier polarity selection on a monolayer tungsten diselenide channel. Nano Lett, 2024, 24(29), 8880

[7] Ghosh S, Sadaf M U K, Graves A R, et al. High-performance p-type bilayer WSe_2 field effect transistors by nitric oxide doping. Nat Commun, 2025, 16, 5649

[8] Wang Y, Kim J C, Li Y, et al. P-type electrical contacts for 2D transition-metal dichalcogenides. Nature, 2022, 610, 61

[9] Das M, Sen D, Sakib N U, et al. High-performance p-type field-effect transistors using substitutional doping and thickness control of two-dimensional materials. Nat Electron, 2025, 8, 24

[10] Zhao S W, Huang J Q, Crépel V, et al. Fractional quantum Hall phases in high-mobility n-type molybdenum disulfide transistors. Nat Electron, 2024, 7, 1117

[11] Chou A S, Lin Y T, Li M Y, et al. Performance step-up in PMOS with monolayer WSe_2 channel. Symp VLSI Technology, 2025

[12] Jaikissoon M, Buragohain P, Mortelmans W, et al. Record PMOS WSe_2 GAA performance using contact planarization, and systematic exploration of manufacturable, high-yield contacts. Symp VLSI Technology, 2025

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