Observation of N-Shaped Negative Differential Resistance in GaAs-Based Modulation-Doped Field Effect Transistor with InAs Quantum Dots

Yueqiang Li[1], Xiaodong Wang[1*], Xiaona Xu[1], Wen Liu[1], Yanling Chen[1],
Fuhua Yang[1,2], Pingheng Tan[2], and Yiping Zeng[3]

[1] *Engineering Research Center for Semiconductor Integrated Technology, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China*
[2] *The State Key Laboratory for Superlattices and Microstructures, Chinese Academy of Sciences, Beijing 100083, China*
[3] *Key Laboratory of Semiconductor Materials Science, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China*

Received May 26, 2010; accepted July 10, 2010; published online October 20, 2010

N-shaped negative differential resistance (NDR) with a high peak-to-valley ratio (PVR) is observed in a GaAs-based modulation-doped field effect transistor (MODFET) with InAs quantum dots (QDs) in the barrier layer (QDFET) compared with a GaAs MODFET. The NDR is explained as the real-space transfer (RST) of high-mobility electrons in a channel into nearby barrier layers with low mobility, and the PVR is enhanced dramatically upon inserting the QD layer. It is also revealed that the QD layer traps holes and acts as a positively charged nano-floating gate after a brief optical illumination, while it acts as a negatively charged nano-floating gate and depletes the adjacent channel when charged by the electrons. The NDR suggests a promising application in memory or high-speed logic devices for the QDFET structure. © 2010 The Japan Society of Applied Physics

DOI: 10.1143/JJAP.49.104002

1. Introduction

Low-dimensional nano structure such as quantum dots (QDs) and quantum wires have gained much interest in solid-state physics and quantum device engineering.[1] In particular, InAs QDs formed in the self-assembled growth mode are attracting intense attention because they provide a convenient method of fabricating high-quality nano scaled QDs. This technique makes it easy to integrate III–V semiconductor devices with QDs.[2,3] Recently, there has been considerable interest in the heterojunction field effect transistor (FET) with InAs QD layers for new applications such as memory elements, single photodetectors, and spin and single electron FETs.[4–15] These QDs located near two-dimensional electron gas (2DEG) channels have been found to act as scattering centers when they are charged by electrons, greatly reducing the mobility of the FET.[4–7] The electrons trapped in the QDs can be eliminated by photo-excited holes, so the resistance of the 2DEG is extremely sensitive to optical illumination. Yusa and Sakaki found that the concentration of 2DEG at a given voltage is persistently increased by light illumination in a modulation doped FET (MODFET) with a layer of dots placed more than 100 nm away from the electron channel, because of the trapping of holes by QDs.[5] Shields *et al.* reported an optically induced enhancement of the 2DEG mobility in a similar MODFET in which a layer of InAs QDs was grown and separated from the 2DEG channel by only a 10 nm $Al_{0.33}Ga_{0.67}As$ barrier, because the illumination reduces the number of electrons trapped in the QDs, lowering their potential.[7] However, relatively little work has been done to identify the influence of QDs on the output characteristics of the QDFET, in spite of their potential for controlling the conventional FET via an operation of a single electron in QDs. Only Wang *et al.*[8] and Phillips *et al.*[10] studied the output characteristics of the QDFETs and found additional transport through the InAs QDs. However, these devices are operated at low voltages.

Furthermore, it has been reported that when a high electric field is applied parallel to the interface of a modulation-doped heterojunction, the high mobility electrons in the narrow bandgap will be heated to energies far above their thermal equilibrium values and may propagate into the adjacent broad bandgap layers.[16] This phenomenon is called real-space transfer (RST) and is used to obtain negative differential resistance and tuned oscillation.[17–23] To our knowledge, the effect of an inserted QD layer on the RST characteristic of a MODFET structure still remains unrevealed.

In this study, we investigate the output characteristics of a QDFET at relatively high voltages. Negative differential resistance (NDR) has been found both in a MODFET and a QDFET, while it is more pronounced in the QDFET. The NDR observed in the QDFET is interpreted on the basis of a RST model, and is further proved by testing of the devices after a brief optical illumination.

2. Experimental Procedure

Samples were grown by GEN II molecular-beam epitaxy (MBE) on a semi-insulating (100)-oriented GaAs substrate. The QDFET structure consists of $GaAs/Al_{0.3}Ga_{0.7}As$ buffer layers, a 40 nm $Al_{0.3}Ga_{0.7}As$ modulated layer (Si, $1 \times 10^{18}/cm^3$), a 20 nm $Al_{0.3}Ga_{0.7}As$ spacer layer, a 20 nm GaAs channel, a 10 nm AlAs barrier, 2 nm GaAs, a thin InAs layer that forms the QDs, 60 nm $Al_{0.3}Ga_{0.7}As$, and a 30 nm GaAs capping layer (Si, $1 \times 10^{18}/cm^3$). The AlAs layer is expected to supply higher localized energy than does a commonly used GaAs barrier. For comparison, another reference sample (FET) was grown with a similar structure except for the InAs QD layer.

The FETs with a 1.0 μm gate were fabricated by standard photolithography and chemical etching. GeAuNiAu/Au were evaporated on an n^+ GaAs capping layer and annealed at 420 °C to form an ohmic contact. 50 nm NiCr was evaporated on $Al_{0.3}Ga_{0.7}As$ to form a Schottky gate. Structures were prepared with a mesa of $4 \times 20\,\mu m^2$. Figure 1(a) shows a schematic diagram and the band structure of the QDFET device. Figure 1(b) shows a plot of the photoluminescence (PL) spectrum recorded on an unprocessed wafer at room temperature. The PL peak is similar to that usually reported for InAs QDs (~1.1 eV).[7] The QDs density is determined to be about $2.42 \times 10^{10}/cm^2$ by imaging an uncapped sample [as shown in the inset of

*E-mail address: xdwang@semi.ac.cn

 © 2010 The Japan Society of Applied Physics

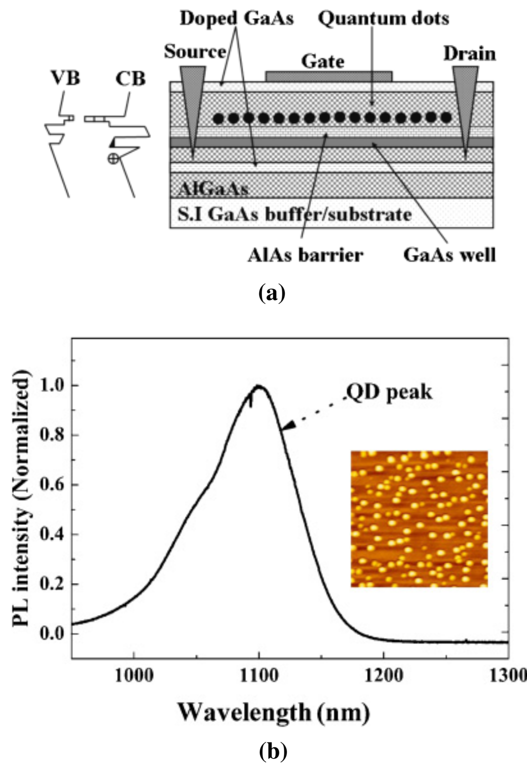


Fig. 1. (Color online) (a) Schematic diagrams of the composition and band structure of the QDFET. CB and VB denote the conduction and valence bands, respectively. (b) Room-temperature PL spectrum and AFM image of QDs.

Fig. 1(b)] with an atomic force microscope (AFM). The fabricated devices were then mounted on a Lakeshore CR6-4K closed-cycle refrigerator-based cryogenic probe station and the *I*–*V* characteristics were measured with an Agilent B1500A semiconductor parameter analyzer.

3. Results and Discussion

Figure 2 shows the output characteristics (I_D–V_{DS}) of a QDFET (solid lines) and a FET without the QD layer (dash lines) at room temperature. The behavior of the QDFET is similar to that of an n-type normally-on transistor with the same threshold voltage of −5.5 V as the FET without a QD layer. The current I_{DS} displays an almost linear increase with V_{DS} in the resistive region, and a very slow increase in the saturation region even at high drain voltages. Obviously, the saturation current of QDFET is much smaller than that of the FET at the same gate bias and drain voltage. This is because the inserted QD layer decreases the electron mobility in 2DEG at room temperature, as reported by other researchers.[8,11] No NDR is observed in either transistor until V_{DS} reaches 12.0 V at room temperature.

Figure 3 shows the output characteristics (I_D–V_{DS}) of the QDFET and FET at 5 K. In this measurement, samples were initially illuminated by a red LED ($\lambda \sim 650$ nm) to liberate electrons unintentionally trapped in QDs and on DX centres,[9] then the drain voltage was scanned from 0 to 12.0 V in the dark. N-shaped NDR can be observed for both devices, while QDFET shows a very distinct peak-to-valley ratio (PVR), as shown in Fig. 3(a). The curves can be reproduced over many cycles of illumination and drain voltage. For QDFET, the NDR characteristic is enhanced by

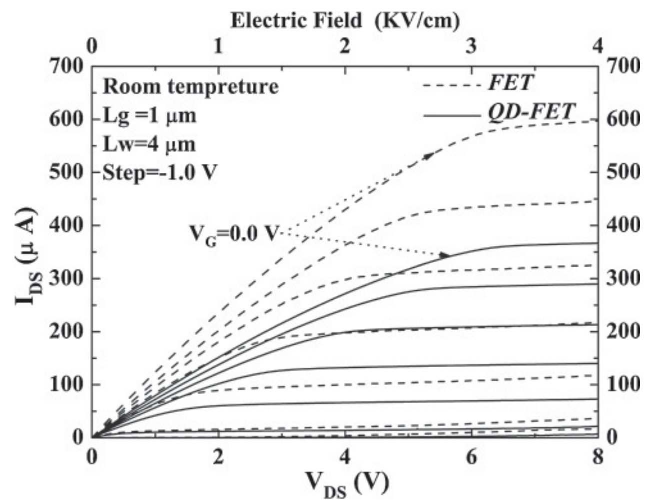
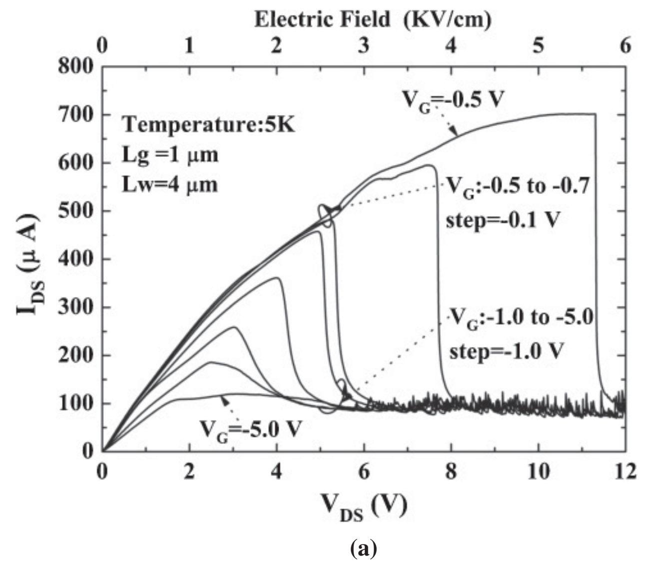


Fig. 2. Output characteristics (I_D–V_{DS}) for 1 μm gate QDFET (solid lines) and FET without embedded QDs (dash lines) measured at room temperature as a function of the drain voltage at different gate biases.



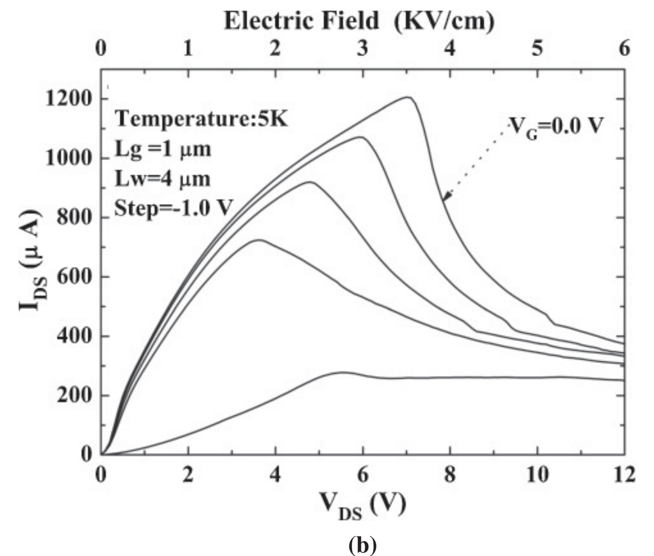


Fig. 3. Output characteristics (I_D–V_{DS}) for 1 μm gate QDFET (a) and FET without embedded QDs (b) at 5 K in the dark. Each curve was recorded after the initial illumination of the device.

 © 2010 The Japan Society of Applied Physics

increasing the gate bias, and it is still considerable when V_G is as low as -4.0 V. The PVR is about 5.47 at $V_G = -1.0$ V and $V_{DS} = 4.93$ V, and the maximum PVR measured is about 7.0 at $V_G = -0.5$ V and $V_{DS} = 11.28$ V. The valley current at a high drain voltage (e.g., $V_{DS} = 12.0$ V) is nearly independent of the applied gate bias. However, the NDR of FET shown in Fig. 3(b) is much weaker than that of the QDFET, and it almost disappears when $V_G = -4.0$ V. The PVR is about 3.1 at $V_G = -1.0$ V and $V_{DS} = 5.9$ V, and the maximum PVR measured is 3.3 at $V_G = 0.0$ V and $V_{DS} = 7.0$ V. Furthermore, the valley current at a high drain voltage increases with gate bias, which is also different from the QDFET. Obviously the NDR characteristics are enhanced in QDFET compared with FET, particularly in the range of V_G from -0.7 to -0.5 V.

The NDR phenomenon in the output characteristics of a MODFET with inserted QDs was reported by Phillips *et al.*, and distinct steps related to the NDR were also observed in the transfer characteristics at the same time.[10] In their study, the channel as well as the QDs are modulation doped by the Si dopants in the $Al_{0.15}Ga_{0.85}As$ layer, and owing to the small separation (2.5 nm $Al_{0.15}Ga_{0.85}As$), the electronic states in the quantum well and the quantum dot layer are coupled. The QDs act as an additional conduction channel, which is different from our QDFET structure. The NDR and the steps observed in the I–V characteristics are attributed to conduction through the bound states in the quantum dots.

We also measured the transfer characteristics of our QDFET at low temperatures, as shown in Fig. 4(a). Following a brief illumination of about 5 s of the device with a red LED, the I_{DS} traces the upper curve, and after the gate voltage has been swept to $+0.75$ V, the I_{DS} traces the lower curve on the reverse sweep. Thus there are two different values of the I_{DS} at the same gate voltage, depending on the illumination and applied gate bias. However, no I_{DS} steps can be observed over a wide range of voltages. This indicates that the NDR phenomenon recorded in our measurement may be induced by other mechanisms. Figure 4(b) shows the transfer characteristics of the FET. The forward and reverse curves almost coincide with each other.

Actually, the QD layer plays a different role in our structure compared with the device mentioned in Phillips *et al.*'s research,[10] as it is placed above the modulation doped layer and separated from the quantum well by a thicker (10 nm) AlAs barrier layer. Research on similar heterostructures have revealed that the QDs here do not participate in the conduction but act as nano-floating gates.[5,7] The conductance of the channel is strongly affected by the layer of QDs. If holes are trapped, the QDs acting as positively charged nano-floating gates lower the potential in the adjacent 2DEG layer, inducing a large increase in mobility and electron density, resulting in relatively high conductance. On the contrary, if electrons are trapped, the QDs play the opposite role, resulting in relatively low conductance. In our test, after the illumination, the photo-excited holes are trapped by the QDs;[5] whereas after the gate voltage has been swept to $+0.75$ V, a low current will flow between the gate and 2DEG and electrons will be captured by the QDs.[5,7] That is the reason for the current bistability observed in the QDFET and illustrated in Fig. 4(a).

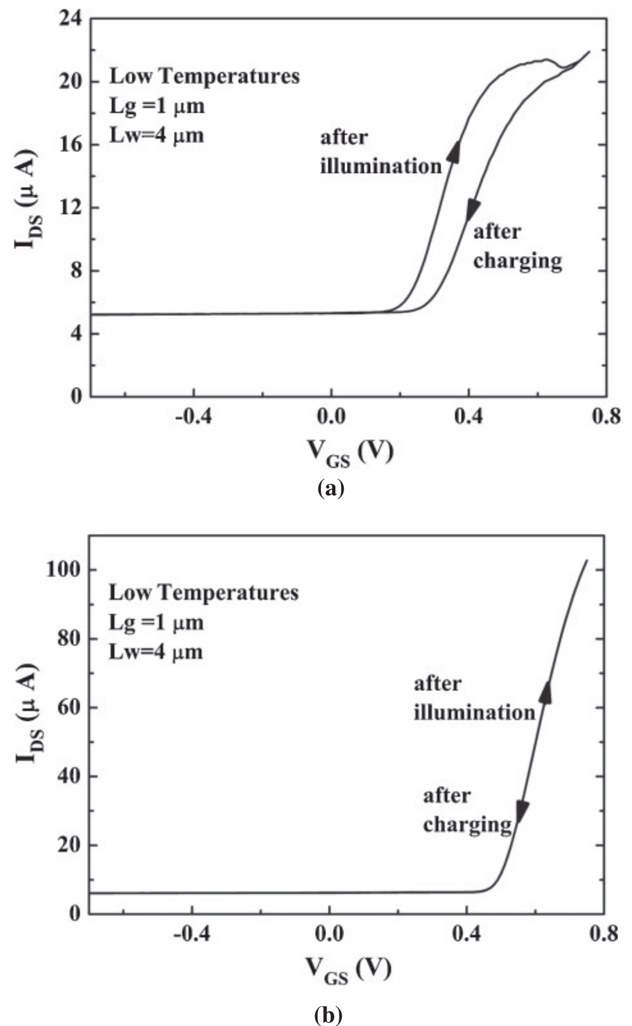


Fig. 4. Transfer characteristics (I_D–V_G) for 1 μm gate QDFET (a) and FET without embedded QDs (b) at low temperatures after a brief illumination at 0 V, the gate voltage is swept from -0.7 to $+0.75$ V and back to -0.7 V at $V_{DS} = 50$ mV.

On the other hand, the NDR of the FET depicted in Fig. 3(b) can be considered to be a common characteristic in modulation doped structures at high electric field.[19–23] It is mainly attributed to the RST of channel electrons.[16] Under the equilibrium condition of the modulation doped GaAs/$Al_xGa_{1-x}As$ heterostructures, the electrons will transfer from their donors in the $Al_xGa_{1-x}As$ to the nearby undoped GaAs layer where they undergo a large reduction in ionized-impurity scattering. The inserted spacer layer will further decrease the scattering. This greatly enhances the mobility, particularly at low temperatures where ionized-impurity scattering is the dominant scattering mechanism in GaAs. When a bias or electric field is applied parallel to the layer interface, the high mobility electrons will be heated to the energies much higher than the thermal equilibrium values. If the electrons acquire enough energy comparable to that of the GaAs–$Al_xGa_{1-x}As$ conduction band discontinuity ΔE_C from the high electric field, the electrons can be injected into the adjacent $Al_xGa_{1-x}As$ layers. The mobility in the $Al_xGa_{1-x}As$ layer ($\leq 500\,cm^2 \cdot V^{-1} \cdot s^{-1}$) is usually much lower than that in the GaAs layer ($\geq 5000\,cm^2 \cdot V^{-1} \cdot s^{-1}$), but the total electron number is constant under a fixed gate bias, so the effect of conductivity in the channel is decreased,

© 2010 The Japan Society of Applied Physics

which is manifested as NDR in the *I–V* characteristics. The PVR is determined by the magnitude of the electron densities and the ratio of mobility between the high- and low-mobility layers.

On the basis of the above analysis, we conclude that the enhancement of NDR in a QDFET can be ascribed to the following mechanism. After the initial illumination of the device by a red LED, the QD layer in which photoexcited holes are trapped acts as positively charged nano-floating gates, resulting in relatively high conductance.[5,7] When the electric field exceeds the threshold value, which is necessary to cause RST, part of the electrons in the channel acquire sufficient energy and move to the modulation doped $Al_{0.3}Ga_{0.7}As$ layers; at the same time, some electrons may gain greater energy by electron–electron collision in the field direction,[16] so it is possible for these electrons to overcome the AlAs barrier and be emitted to the upper AlAs/InAs QDs/$Al_{0.3}Ga_{0.7}As$ layers. The electrons entering the upper layers lose their energies through phonon emission and will be trapped in the QDs sandwiched by the large band-gap $Al_{0.3}Ga_{0.7}As$ and AlAs layers.[17] As has been mentioned before, these trapped electrons will act as negatively charged nano-floating gates that greatly reducing the 2DEG mobility. The superposition of these two effects results in more pronounced NDR in QDFET, as depicted in Fig. 3(a).

Furthermore, the valley current of the QDFET at high V_{DS} is nearly independent of the applied gate bias, which is different from the FET. It indicates that when NDR occurs, the channel will go into a low-mobility state that is insensitive to the gate potential. The QD layer is the only difference between the QDFET and FET, so we believe that the low-mobility state is just due to the negatively charged QDs after the NDR has happened.

To further illustrate the effect of the inserted QD layer, and particularly the reason for high PVR in the QDFET, the I_{DS}–V_{DS} characteristics of the same QDFET and FET were measured at $V_G = -1.0$ V under different initial conditions. As shown in Fig. 5, the solid lines were recorded after an initial illumination of the device, and the dashed lines were recorded after the gate bias was maintained at 1.5 V for about 5 s. As we expect, the I_{DS}–V_{DS} lines of the FET measured under these two initial conditions [Fig. 5(b)] almost coincide with each other because no QDs are embedded, while the results of the QDFET show great differences. In Fig. 5(a), the significantly lower peak value of the dashed line indicates that the charge states of the QDs can greatly affect the NDR effect. As previously mentioned after illumination the QDs will be filled with holes, however, if prior to the measurement the gate bias is set to 1.5 V for about 5 s, electrons will be trapped there. The trapped electrons under this situation act as negatively charged nano-floating gates or neutralize some of the holes previously trapped by the QDs, so the QD layer depletes the channel, as mentioned above, and the peak value of I_{DS} decreases markedly. The V_{NDR} at which NDR arises shifts to a low voltage from 4.93 to 3.29 V, and the PVR drops from 5.30 to 2.06, but the valley currents remain almost the same as at the high V_{DS}, which means the device will reach the same equilibrium state as at high V_{DS} even if it is operated under different initial conditions. Therefore, we experimentally demonstrated that the PVR and peak value of a QDFET are determined by the charge states of the QDs. The high PVR is induced by the holes trapped in the QD layer after illumination.

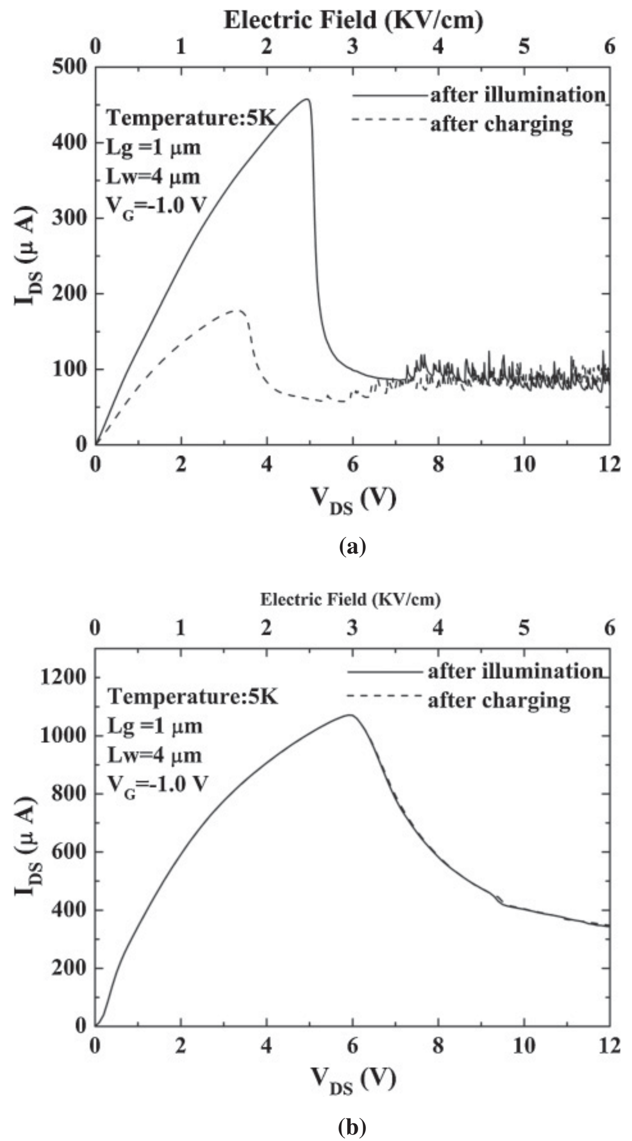


Fig. 5. Output characteristics (I_D–V_{DS}) for 1 μm gate QDFET (a) and FET (b) at 5 K in the dark under different initial conditions of illumination and charging.

As we know, very short switching time between the high- and low-mobility layers has been confirmed by other researchers in similar devices.[17,20] In consideration of the pronounced NDR that we observed, the QDFET may be an attractive candidate for high-speed logic applications and memory devices. The predicted high hole-localization energy (~1.4 eV) in GaSb/AlAs QDs also makes it possible for the device to be operated at room temperature.[12]

4. Conclusions

In summary, we investigated the output characteristics of QDFET and FET without an embedded InAs QD layer. Both transistors exhibited N-shaped NDR at low temperatures, which was attributed to the RST of hot carriers in a channel into nearby barrier layers. The NDR characteristics of the QDFET were enhanced dramatically compared with those of the FET without the embedded QD layer, and the

 © 2010 The Japan Society of Applied Physics

pronounced NDR characteristic with high PVR (∼7.0) was clearly observed. After a brief optical illumination, the QD layer traps holes and acted as positively charged floating gates. When NDR arises, some of the real-space-transferred hot electrons propagated into the QD layer, recombined with the holes and were then trapped there. This drastically lowered the mobility in the 2DEG channel and caused a the sharp decrease in the drain current. When the QD layer was charged by the electrons via the gate bias, it acted as a negatively charged nano-floating gate and depleted the adjacent channel. Our results indicated that the QDFET can be an attractive candidate for high-speed logic application and memory devices.

Acknowledgements

The authors greatly acknowledge the support from the National Basic Research Program of China (973 Program) under the grant number 2010CB934104, and National Natural Science Foundation of China under the grant number of 60606024.

1) D. Bimberg, M. Grundmann, and N. N. Ledentsov: *Quantum Dot Heterostructures* (Wiley, New York, 1998).
2) D. Leonard, M. Krishnamurthy, C. M. Reaves, S. P. Denbaars, and P. M. Petroff: Appl. Phys. Lett. **63** (1993) 3203.
3) J. M. Moison, F. Houzay, F. Barthe, L. Leprince, E. Andre, and O. Vatel: Appl. Phys. Lett. **64** (1994) 196.
4) H. Son, J. Kim, M. Kim, and S. Hong: Jpn. J. Appl. Phys. **40** (2001) 2801.
5) G. Yusa and H. Sakaki: Appl. Phys. Lett. **70** (1997) 345.
6) E. Ribeiro, E. Muller, T. Heinzel, H. Auderest, K. Ensslim, G. Medeiros-Ribeiro, and P. M. Petroff: Phys. Rev. B **58** (1998) 1506.
7) A. J. Shields, M. P. O'Sullivan, I. Farrer, D. A. Ritchie, K. Cooper, C. L. Foden, and M. Pepper: Appl. Phys. Lett. **74** (1999) 735.
8) T. H. Wang, H. W. Li, and J. M. Zhou: Appl. Phys. Lett. **82** (2003) 3092.
9) A. J. Shields, M. P. O'Sullivan, I. Farrer, D. A. Ritchie, M. L. Leadbeater, N. K. Patel, R. A. Hogg, C. E. Norman, N. J. Curson, and M. Pepper: Jpn. J. Appl. Phys. **40** (2001) 2058.
10) J. Phillips, K. Kamath, T. Brock, and P. Bhattacharya: Appl. Phys. Lett. **72** (1998) 3509.
11) C. Balocco, A. M. Song, and M. Missous: Appl. Phys. Lett. **85** (2004) 5911.
12) A. Marent, M. Geller, A. Schliwa, D. Feise, K. Pötschke, and D. Bimberg: Appl. Phys. Lett. **91** (2007) 242109.
13) M. Geller, A. Marent, T. Nowozin, D. Bimberg, N. Akçay, and N. Öncan: Appl. Phys. Lett. **92** (2008) 092108.
14) S. Kashiwada, T. Matsuda, and K. Yoh: J. Cryst. Growth **301–302** (2007) 785.
15) K. Yoh and H. Kazama: Physica E **7** (2000) 440.
16) K. Hess, H. Morkoc, H. Shichijo, and B. G. Streetman: Appl. Phys. Lett. **35** (1979) 469.
17) M. Keever, K. Hess, and M. Ludowise: IEEE Electron Device Lett. **3** (1982) 297.
18) R. Sakamoto, K. Akai, and M. Inoue: IEEE Trans. Electron Devices **36** (1989) 2344.
19) C. L. Wu and W. C. Hsu: IEEE Trans. Electron Devices **43** (1996) 207.
20) S. J. Kim, T. Sugaya, M. Ogura, Y. Sugiyama, and K. Tomizawa: Physica B **272** (1999) 117.
21) Y. W. Chen, W. C. Hsu, H. M. Shieh, Y. J. Chen, Y. S. Lin, Y. J. Li, and T. B. Wang: IEEE Trans. Electron Devices **49** (2002) 221.
22) T. Sugaya, K. Y. Jang, C. K. Hahn, M. Ogura, K. Komori, A. Shinoda, and K. Yonei: J. Appl. Phys. **97** (2005) 034507.
23) M. L. Orlov and K. L. Orlov: Semiconductors **43** (2009) 652.

 © 2010 The Japan Society of Applied Physics